Chapter 1 Power Electronic Systems

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Power Electronic Systems

- Block diagram
- Role of Power Electronics
- Reasons for growth

Figure 1-1 Block diagram of a power electronic system.
Linear Power Supply

- Series transistor as an adjustable resistor
- Low Efficiency
- Heavy and bulky
Switch-Mode Power Supply

- Transistor as a switch
- High Efficiency
- High-Frequency Transformer

Figure 1-3  Switch-mode dc power supply.
Basic Principle of Switch-Mode Synthesis

- Constant switching frequency
- Pulse width controls the average
- L-C filters the ripple

Figure 1-4  Equivalent circuit, waveforms, and frequency spectrum of the supply in Fig. 1-3.
Application in Adjustable Speed Drives

- Conventional drive wastes energy across the throttling valve to adjust flow rate
- Using power electronics, motor-pump speed is adjusted efficiently to deliver the required flow rate

Figure 1-5  Energy conservation: (a) conventional drive, (b) adjustable-speed drive.
Scope and Applications

<table>
<thead>
<tr>
<th>TABLE 1-1 Power Electronic Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a) Residential</td>
</tr>
<tr>
<td>- Refrigeration and freezers</td>
</tr>
<tr>
<td>- Space heating</td>
</tr>
<tr>
<td>- Air conditioning</td>
</tr>
<tr>
<td>- Cooking</td>
</tr>
<tr>
<td>- Lighting</td>
</tr>
<tr>
<td>- Electronics (personal computers,</td>
</tr>
<tr>
<td>other entertainment equipment)</td>
</tr>
<tr>
<td>(b) Commercial</td>
</tr>
<tr>
<td>- Heating, ventilating, and air</td>
</tr>
<tr>
<td>conditioning</td>
</tr>
<tr>
<td>- Central refrigeration</td>
</tr>
<tr>
<td>- Lighting</td>
</tr>
<tr>
<td>- Computers and office equipment</td>
</tr>
<tr>
<td>- Uninterruptible power supplies (UPSs)</td>
</tr>
<tr>
<td>- Elevators</td>
</tr>
<tr>
<td>(c) Industrial</td>
</tr>
<tr>
<td>- Pumps</td>
</tr>
<tr>
<td>- Compressors</td>
</tr>
<tr>
<td>- Blowers and fans</td>
</tr>
<tr>
<td>- Machine tools (robots)</td>
</tr>
<tr>
<td>- Arc furnaces, induction furnaces</td>
</tr>
<tr>
<td>- Lighting</td>
</tr>
<tr>
<td>- Industrial lasers</td>
</tr>
<tr>
<td>- Induction heating</td>
</tr>
<tr>
<td>- Welding</td>
</tr>
<tr>
<td>(d) Transportation</td>
</tr>
<tr>
<td>- Traction control of electric vehicles</td>
</tr>
<tr>
<td>- Battery chargers for electric vehicles</td>
</tr>
<tr>
<td>- Electric locomotives</td>
</tr>
<tr>
<td>- Street cars, trolley buses</td>
</tr>
<tr>
<td>- Subways</td>
</tr>
<tr>
<td>- Automotive electronics including</td>
</tr>
<tr>
<td>engine controls</td>
</tr>
<tr>
<td>(e) Utility systems</td>
</tr>
<tr>
<td>- High-voltage dc transmission (HVDC)</td>
</tr>
<tr>
<td>- Static var compensation (SVC)</td>
</tr>
<tr>
<td>- Supplemental energy sources (wind,</td>
</tr>
<tr>
<td>photovoltaic), fuel cells</td>
</tr>
<tr>
<td>- Energy storage systems</td>
</tr>
<tr>
<td>- Induced-draft fans and boiler</td>
</tr>
<tr>
<td>- Feedwater pumps</td>
</tr>
<tr>
<td>(f) Aerospace</td>
</tr>
<tr>
<td>- Space shuttle power supply systems</td>
</tr>
<tr>
<td>- Satellite power systems</td>
</tr>
<tr>
<td>- Aircraft power systems</td>
</tr>
<tr>
<td>(g) Telecommunications</td>
</tr>
<tr>
<td>- Battery chargers</td>
</tr>
<tr>
<td>- Power supplies (dc and UPS)</td>
</tr>
</tbody>
</table>

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Power Processor as a Combination of Converters

• Most practical topologies require an energy storage element, which also decouples the input and the output side converters.

Figure 1-6 Power processor block diagram.
Power Flow through Converters

- Converter is a general term
- An ac/dc converter is shown here
- Rectifier Mode of operation when power from ac to dc
- Inverter Mode of operation when power from ac to dc

Figure 1-7  ac-to-dc converters.
AC Motor Drive

- Converter 1 rectifies line-frequency ac into dc
- Capacitor acts as a filter; stores energy; decouples
- Converter 2 synthesizes low-frequency ac to motor
- Polarity of dc-bus voltage remains unchanged
  - ideally suited for transistors of converter 2

Figure 1-8  Block diagram of an ac motor drive.
Matrix Converter

- Very general structure
- Would benefit from bi-directional and bi-polarity switches
- Being considered for use in specific applications

Figure 1-9  (a) Matrix converter. (b) Voltage source.
Interdisciplinary Nature of Power Electronics

**Figure 1-10** Interdisciplinary nature of power electronics.
Chapter 2 Overview of Power Semiconductor Devices

Chapter 2 Overview of Power Semiconductor Switches

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Diodes

- On and off states controlled by the power circuit

Figure 2-1 Diode: (a) symbol, (b) $i-v$ characteristic, (c) idealized characteristic.
Diode Turn-Off

- Fast-recovery diodes have a small reverse-recovery time

Figure 2-2  Diode turn-off.
Thyristors

- Semi-controlled device
- Latches ON by a gate-current pulse if forward biased
- Turns-off if current tries to reverse
Figure 2-4  Thyristor: (a) circuit, (b) waveforms, (c) turn-off time interval $t_q$.

- For successful turn-off, reverse voltage required for an interval greater than the turn-off interval $t_q$. 
Generic Switch Symbol

• Idealized switch symbol
• When on, current can flow only in the direction of the arrow
• Instantaneous switching from one state to the other
• Zero voltage drop in on-state
• Infinite voltage and current handling capabilities

Figure 2-5  Generic controllable switch.
Switching Characteristics (linearized)

Switching Power Loss is proportional to:
- switching frequency
- turn-on and turn-off times

Figure 2-6  Generic-switch switching characteristics (linearized): (a) simplified clamped-inductive-switching circuit, (b) switch waveforms, (c) instantaneous switch power loss.
Bipolar Junction Transistors (BJT)

- Used commonly in the past
- Now used in specific applications
- Replaced by MOSFETs and IGBTs

Figure 2-7 A BJT: (a) symbol, (b) i–v characteristics, (c) idealized characteristics.
Various Configurations of BJTs

Figure 2-8  Darlington configurations: (a) Darlington, (b) triple Darlington.
MOSFETs

- Easy to control by the gate
- Optimal for low-voltage operation at high switching frequencies
- On-state resistance a concern at higher voltage ratings

Figure 2-9  N-channel MOSFET: (a) symbol, (b) $i$–$v$ characteristics, (c) idealized characteristics.
Gate-Turn-Off Thyristors (GTO)

- Slow switching speeds
- Used at very high power levels
- Require elaborate gate control circuitry

Figure 2-10 A GTO: (a) symbol, (b) i–v characteristics, (c) idealized characteristics.
GTO Turn-Off

Figure 2-11  Gate turn-off transient characteristics: (a) snubber circuit, (b) GTO turn-off characteristic.

• Need a turn-off snubber
Figure 2-12 An IGBT: (a) symbol, (b) $i$--$v$ characteristics, (c) idealized characteristics.
Figure 2-13 An MCT: (a) circuit symbols, (b) \( i-v \) characteristic, (c) idealized characteristics.
Comparison of Controllable Switches

<table>
<thead>
<tr>
<th>Device</th>
<th>Power Capability</th>
<th>Switching Speed</th>
</tr>
</thead>
<tbody>
<tr>
<td>BJT/MD</td>
<td>Medium</td>
<td>Medium</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Low</td>
<td>Fast</td>
</tr>
<tr>
<td>GTO</td>
<td>High</td>
<td>Slow</td>
</tr>
<tr>
<td>IGBT</td>
<td>Medium</td>
<td>Medium</td>
</tr>
<tr>
<td>MCT</td>
<td>Medium</td>
<td>Medium</td>
</tr>
</tbody>
</table>
Summary of Device Capabilities

Figure 2-14 Summary of power semiconductor device capabilities. All devices except the MCT have a relatively mature technology, and only evolutionary improvements in the device capabilities are anticipated in the next few years. However, MCT technology is in a state of rapid expansion, and significant improvements in the device capabilities are possible, as indicated by the expansion arrow in the diagram.
Chapter 3

Review of Basic Electrical and Magnetic Circuit Concepts

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Symbols and Conventions

- Symbols
- Polarity of Voltages; Direction of Currents
- MKS SI units

Figure 3-1  Instantaneous power flow.
Sinusoidal Steady State

Figure 3-2 Sinusoidal steady state.
Three-Phase Circuit

Figure 3-3 Three-phase circuit.
Figure 3-4  Nonsinusoidal waveforms in steady state.
## Fourier Analysis

### Table 3-1 Use of Symmetry in Fourier Analysis

<table>
<thead>
<tr>
<th>Symmetry</th>
<th>Condition Required</th>
<th>$a_h$ and $b_h$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Even</td>
<td>$f(-t) = f(t)$</td>
<td>$b_h = 0$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$a_h = \frac{2}{\pi} \int_0^\pi f(t) \cos(\omega t) , d(\omega t)$</td>
</tr>
<tr>
<td>Odd</td>
<td>$f(-t) = -f(t)$</td>
<td>$a_h = 0$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$b_h = \frac{2}{\pi} \int_0^\pi f(t) \sin(\omega t) , d(\omega t)$</td>
</tr>
<tr>
<td>Half-wave</td>
<td>$f(t) = -f(t + \frac{T}{2})$</td>
<td>$a_h = b_h = 0$ for even $h$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$a_h = \frac{2}{\pi} \int_0^\pi f(t) \cos(\omega t) , d(\omega t)$ for odd $h$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$b_h = \frac{2}{\pi} \int_0^\pi f(t) \sin(\omega t) , d(\omega t)$ for odd $h$</td>
</tr>
<tr>
<td>Even quarter-wave</td>
<td>Even and half-wave</td>
<td>$b_h = 0$ for all $h$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$a_h = \begin{cases} \frac{4}{\pi} \int_0^{\pi/2} f(t) \cos(\omega t) , d(\omega t) &amp; \text{for odd } h \ 0 &amp; \text{for even } h \end{cases}$</td>
</tr>
<tr>
<td>Odd quarter-wave</td>
<td>Odd and half-wave</td>
<td>$a_h = 0$ for all $h$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$b_h = \begin{cases} \frac{4}{\pi} \int_0^{\pi/2} f(t) \sin(\omega t) , d(\omega t) &amp; \text{for odd } h \ 0 &amp; \text{for even } h \end{cases}$</td>
</tr>
</tbody>
</table>
Distortion in the Input Current

Figure 3-5  Line-current distortion.

- Voltage is assumed to be sinusoidal
- Subscript “1” refers to the fundamental
- The angle is between the voltage and the current fundamental
Figure 3-6 Phasor representation.
Response of $L$ and $C$

**Figure 3-7** Inductor and capacitor response.
Inductor Voltage and Current in Steady State

- Volt-seconds over $T$ equal zero.

Figure 3-8  Inductor response in steady state.
Capacitor Voltage and Current in Steady State

- Amp-seconds over $T$ equal zero.

Figure 3-9 Capacitor response in steady state.
Ampere’s Law

- Direction of magnetic field due to currents
- Ampere’s Law: Magnetic field along a path

Figure 3-10  (a) General formulation of Ampere’s law. (b) Specific example of Ampere’s law in the case of a winding on a magnetic core with an airgap.
Figure 3-11 Determination of the magnetic field direction via the right-hand rule in (a) the general case and (b) a specific example of a current-carrying coil wound on a toroidal core.
$B-H$ Relationship; Saturation

![Diagram of B-H Relationship]

**Figure 3-12** Relation between $B$- and $H$-fields.

- Definition of permeability

\[
\begin{align*}
\mu & = \frac{\Delta B}{\Delta H} = \frac{B}{H} \\
\mu_\Delta & = \frac{\Delta B}{\Delta H}
\end{align*}
\]
Continuity of Flux Lines

\[ \phi_1 + \phi_2 + \phi_3 = 0 \]

**Figure 3-13** Continuity of flux.
Concept of Magnetic Reluctance

- Flux is related to ampere-turns by reluctance

\[ R = \frac{l}{\mu A} \quad \phi = \frac{Ni}{R} \]

**Figure 3-14** Magnetic reluctance.
## Analogy between Electrical and Magnetic Variables

### Table 3-2 Electrical–Magnetic Analogy

<table>
<thead>
<tr>
<th>Magnetic Circuit</th>
<th>Electric Circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td>mmf $Ni$</td>
<td>$v$</td>
</tr>
<tr>
<td>Flux $\phi$</td>
<td>$i$</td>
</tr>
<tr>
<td>reluctance $R$</td>
<td>$R$</td>
</tr>
<tr>
<td>permeability $\mu$</td>
<td>$1/\rho$, where $\rho =$ resistivity</td>
</tr>
</tbody>
</table>
Analogy between Equations in Electrical and Magnetic Circuits

**Table 3-3 Magnetic—Electrical Circuit Equation Analogy**

<table>
<thead>
<tr>
<th>Magnetic</th>
<th>Electrical (dc)</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \frac{N_i}{\phi} = R = \frac{l}{\mu A} )</td>
<td>Ohm’s law: ( \frac{\nu}{i} = R = \frac{l}{A/\rho} )</td>
</tr>
<tr>
<td>( \phi \sum_k R_k = \sum_m N_m i_m )</td>
<td>Kirchhoff’s voltage law: ( i \sum_k R_k = \sum_m \nu_m )</td>
</tr>
<tr>
<td>( \sum \phi_k = 0 )</td>
<td>Kirchhoff’s current law: ( \sum_i i_k = 0 )</td>
</tr>
</tbody>
</table>
Magnetic Circuit and its Electrical Analog

Figure 3-15  (a) Magnetic circuit. (b) An electrical analog.
Faraday’s Law and Lenz’s Law

Figure 3-16  (a) Flux direction and voltage polarity.  
(b) Lenz’s law.
Inductance $L$

- Inductance relates flux-linkage to current

Figure 3-17  Self-inductance $L$. 
Analysis of a Transformer

Figure 3-18  (a) Cross section of a transformer. (b) The $B$–$H$ characteristics of the core.
Transformer Equivalent Circuit

Figure 3-19  Equivalent circuit for (a) a physically realizable transformer wound on a lossless core and (b) an ideal transformer.
Including the Core Losses

Figure 3-21  Equivalent circuit of a transformer including the effects of hysteresis loss. (a) Circuit components are on both sides (coil 1 and coil 2 sides) of the ideal transformer. (b) Components from the secondary (coil 2) side are reflected across the ideal transformer to the primary (coil 1) side.
Transformer Core Characteristic

Figure 3-20  $B-H$ characteristic of a transformer core having hysteresis and hence magnetic losses.
Chapter 4

Computer Simulation

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System to be Simulated

- Challenges in modeling power electronic systems

Figure 4-1  Power electronics system: a block diagram.
Large-Signal System Simulation

- Simplest component models

![Diagram of a power system with labeled components](image-url)

**Figure 4-2** Open-loop, large-signal simulation.
Small-Signal Linearized Model for Controller Design

- System linearized around the steady-state point

Figure 4-3 Small-signal (linear) model and controller design.
Closed-Loop Operation: Large Disturbances

- Simplest component models
- Nonlinearities, Limits, etc. are included

Figure 4-4 Closed-loop, large-signal system behavior.
Modeling of Switching Operation

- Detailed device models
- Just a few switching cycles are studied

Figure 4-5 Switching details.
Modeling of a Simple Converter

- Input voltage takes on two discrete values

Figure 4-6  Simplified equivalent circuit of a switch-mode, regulated dc power supply (same as in Fig. 1-3).
Trapezoidal Method of Integration

The area shown above represents the integral

Figure 4-7
Trapezoidal method of integration.

- The area shown above represents the integral
A Simple Example

- The input voltage takes on two discrete values

Figure 4-8  (a) Circuit for simulation. (b) Switch control waveform.

- The input voltage takes on two discrete values
Modeling using PSpice

- Schematic approach is far superior

![Diagram](image)

**PSpice Example**

```plaintext
* DIODE 2 1 POWER_DIODE
RSnub 1 5 100.0
CSnub 5 2 0.1uF
*
SW 2 0 6 0 SWITCH
VCNTL 6 0 PULSE(0V,1V,0s,1ns,1ns,7.5us,10us)
*
L 1 3 5uH IC=4A
rL 3 4 1m
C 4 2 100uF IC=5.5V
RLOAD 4 2 1.0
*
VD 1 0 8.0V
*
.MODEL POWER_DIODE D(RS=0.01,CJO=10pF)
.MODEL SWITCH VSWITCH(RON=0.01)
.TRAN 10us 500.0us 0s 0.2us uic
.PROBE
.END
```

**Figure 4-9** PSpice simulation of circuit in Fig. 4-8.
PSpice-based Simulation

Figure 4-10  Results of PSpice simulation: \( i_L \) and \( v_c \).

- Simulation results
Simulation using MATLAB

```matlab
% Solution of the Circuit in Fig. 4-6 using Trapezoidal Method of Integration.
clear all

% Input Data
Vd=5; L=5e-6; C=100e-6; rL=1e-3; R=1.0; fs=100e3; Vcontrol=0.75;
Ts=1/fs; tmax=50*Ts; deltat=Ts/50;

% time= 0:deltat:time;
for il=1:tmax
  time= time + deltat;
  % Solution
  x = M * [il(k-1) vC(k-1)]' + N * (voil(k) + voil(k-1));
  il(k) = x(1); vC(k) = x(2);
end
```

**Figure 4-11** MATLAB simulation of circuit in Fig. 4-6.
MATLAB-based Simulation

- Simulation results

Figure 4-12 MATLAB simulation results.
Chapter 5
Diode Rectifiers

Chapter 5  Line-Frequency Diode Rectifiers: Line-Frequency ac → Uncontrolled dc

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Diode Rectifier Block Diagram

- Uncontrolled utility interface (ac to dc)
A Simple Circuit

Figure 5-2 Basic rectifier with a load resistance.

- Resistive load
A Simple Circuit (\(R-L\) Load)

- Current continues to flows for a while even after the input voltage has gone negative
A Simple Circuit (Load has a dc back-emf)

- Current begins to flow when the input voltage exceeds the dc back-emf
- Current continues to flows for a while even after the input voltage has gone below the dc back-emf
Single-Phase Diode Rectifier Bridge

- Large capacitor at the dc output for filtering and energy storage

Figure 5-5  Single-phase diode bridge rectifier.
Diode-Rectifier Bridge Analysis

Figure 5-6  Idealized diode bridge rectifiers with $L_s = 0$.

- Two simple (idealized) cases to begin with
Redrawing Diode-Rectifier Bridge

- Two groups, each with two diodes

Figure 5-7 Redrawn rectifiers of Fig. 5-6.
Waveforms with a purely resistive load and a purely dc current at the output

- In both cases, the dc-side voltage waveform is the same
Diode-Rectifier Bridge Input Current

Figure 5-9  Line current $i_s$ in the idealized case.

- Idealized case with a purely dc output current
Diode-Rectifier Bridge Analysis with AC-Side Inductance

Figure 5-10  Single-phase rectifier with $L_s$.

- Output current is assumed to be purely dc
Understanding Current Commutation

Figure 5-11  Basic circuit to illustrate current commutation. Waveforms assume $L_s = 0$.

- Assuming inductance in this circuit to be zero
Understanding Current Commutation (cont.)

Figure 5-12  (a) Circuit during the commutation. (b) Circuit after the current commutation is completed.

• Inductance in this circuit is included
Current Commutation Waveforms

\begin{align*}
\text{Area } A_u \\
v_L \\
0 \\
in \\
0 \\
0 \\
\end{align*}

\textit{Figure 5-13} Waveforms in the basic circuit of Fig. 5-11. Note that a large value of } L_s \text{ is used to clearly show the commutation interval.}

• Shows the volt-seconds needed to commutate current
Current Commutation in Full-Bridge Rectifier

- Shows the necessary volt-seconds

Figure 5-14  (a) Single-phase diode rectifier with $L_s$. (b) Waveforms.
Understanding Current Commutation

• Note the current loops for analysis

Figure 5-15  Redrawn circuit of Fig. 5-14a during current commutation.
Rectifier with a dc-side voltage

Figure 5-16  (a) Rectifier with a constant dc-side voltage. (b) Equivalent circuit. (c) Waveforms.
DC-Side Voltage and Current Relationship

- Zero current corresponds to dc voltage equal to the peak of the input ac voltage

**Figure 5-17** Normalized $I_d$ versus $V_d$ in the rectifier of Fig. 5-16a with a constant dc-side voltage.
Effect of DC-Side Current on THD, PF and DPF

- Very high THD at low current values

Figure 5-18  Total harmonic distortion, DPF, and PF in the rectifier of Fig. 5-16a with a constant dc-side voltage.
Crest Factor versus the Current Loading

**Figure 5-19** Normalized $V_d$ and the crest factor in the rectifier of Fig. 5-16a with a constant dc-side voltage.

- The Crest Factor is very high at low values of current
Diode-Rectifier with a Capacitor Filter

![Diode Rectifier Circuit Diagram]

**Figure 5-20** Practical diode-bridge rectifier with a filter capacitor.

- Power electronics load is represented by an equivalent load resistance
Diode Rectifier Bridge

- Equivalent circuit for analysis on one-half cycle basis

Figure 5-21  Equivalent circuit of Fig. 5-20.
Diode-Bridge Rectifier: Waveforms

- Analysis using MATLAB

Figure 5-22 Waveforms in the circuit of Fig. 5-20, obtained in Example 5-1.
Diode-Bridge Rectifier: Waveforms

Figure 5-23  Waveforms in the circuit of Fig. 5-20, obtained in Example 5-2.

- Analysis using PSpice
Input Line-Current Distortion

Figure 5-24  Distorted line current in the rectifier of Fig. 5-20.

• Analysis using PSpice
Line-Voltage Distortion

• PCC is the point of common coupling

Figure 5-25  Line-voltage notching and distortion.
Line-Voltage Distortion

- Distortion in voltage supplied to other loads

Figure 5-26 Voltage waveform at the point of common coupling in the circuit of Fig. 5-25.
Voltage Doubler Rectifier

- In 115-V position, one capacitor at-a-time is charged from the input.

Figure 5-27 Voltage-doubler rectifier.
A Three-Phase, Four-Wire System

- A common neutral wire is assumed

Figure 5-28  Three-phase, four-wire system.
Current in A Three-Phase, Four-Wire System

Figure 5-29 Neutral-wire current $i_n$.

- The current in the neutral wire can be very high
Three-Phase, Full-Bridge Rectifier

Figure 5-30  Three-phase, full-bridge rectifier.

- Commonly used
Three-Phase, Full-Bridge Rectifier: Redrawn

Figure 5-31 Three-phase rectifier with a constant dc current.

- Two groups with three diodes each
Three-Phase, Full-Bridge Rectifier Waveforms

- Output current is assumed to be dc

![Diagram showing waveforms in the circuit of Fig. 5-31.](image)

Figure 5-32 Waveforms in the circuit of Fig. 5-31.
Three-Phase, Full-Bridge Rectifier: Input Line-Current

Figure 5-33 Line current in a three-phase rectifier in the idealized case with \( L_s = 0 \) and a constant dc current.

- Assuming output current to be purely dc and zero ac-side inductance
Three-Phase, Full-Bridge Rectifier

- Including the ac-side inductance

Figure 5-34 Three-phase rectifier with a finite $L_s$ and a constant dc current.
3-Phase Rectifier: Current Commutation

- output current is assumed to be purely dc
Rectifier with a Large Filter Capacitor

Figure 5-36  (a) Three-phase rectifier with a finite $L_s$ and a constant dc voltage. (b) Equivalent circuit. (c) Waveforms.

- Output voltage is assumed to be purely dc
Three-Phase, Full-Bridge Rectifier

Figure 5-37  Total harmonic distortion, DPF, and PF in the rectifier of Fig. 5-36 with a constant dc voltage.

• THD, PF and DPF as functions of load current
Crest Factor versus the Current Loading

Figure 5-38. Normalized $V_d$ and crest factor in the rectifier of Fig. 5-36 with a constant dc voltage.

• The Crest Factor is very high at low values of current.
Three-Phase Rectifier Waveforms

Figure 5-39 Waveforms in the rectifier of Fig. 5-30, obtained in Example 5-7.

• PSpice-based analysis
Chapter 6
Thyristor Converters

Chapter 6  Line-Frequency Phase-Controlled Rectifiers and Inverters: Line-Frequency ac ↔ Controlled dc

6-1 Introduction 121
6-2 Thyristor Circuits and Their Control 122
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• Controlled conversion of ac into dc
Thyristor Converters

- Two-quadrant conversion

Figure 6-1  Line-frequency controlled converter.
Primitive circuits with thyristors

Figure 6-2 Basic thyristor converters.
Thyristor Triggering

- ICs available

Figure 6-3  Gate trigger control circuit.
Full-Bridge Thyristor Converters

- Single-phase and three-phase

Figure 6-4 Practical thyristor converters.
Single-Phase Thyristor Converters

- Two groups with two thyristor each

**Figure 6-5** Single-phase thyristor converter with $L_i = 0$ and a constant dc current.
1-Phase Thyristor Converter Waveforms

- Assuming zero ac-side inductance

Figure 6-6  Waveforms in the converter of Fig. 6-5.
Average DC Output Voltage

- Assuming zero ac-side inductance

**Figure 6-7** Normalized $V_d$ as a function of $\alpha$. 
Input Line-Current Waveforms

- Harmonics, power and reactive power

Figure 6-8 The ac-side quantities in the converter of Fig. 6-5.
1-Phase Thyristor Converter

- Finite ac-side inductance; constant dc output current

*Figure 6-9* Single-phase thyristor converter with a finite $L_s$ and a constant dc current.
Thyristor Converter Waveforms

- Finite ac-side inductance

Figure 6-10 Waveforms in the converter of Fig. 6-9.
Thyristor Converter: Discontinuous Mode

- This mode can occur in a dc-drive at light loads.

Figure 6-11 (a) A practical thyristor converter. (b) Waveforms.
Thyristor Converter Waveforms

Figure 6-12  Waveforms in Example 6-2 for the circuit of Fig. 6-11a.

- PSpice-based simulation
Thyristor Converter Waveforms: Discontinuous Conduction Mode

Figure 6-13 Waveforms in a discontinuous-current-conduction mode.

- PSpice-based simulation
DC Voltage versus Load Current

\[ V_d \] versus \( I_d \) in the single-phase thyristor converter of Fig. 6-11a.

- Various values of delay angle

---

Figure 6-14
Thyristor Converters: Inverter Mode

- Assuming the ac-side inductance to be zero

Figure 6-15  (a) Inverter, assuming a constant dc current. (b) Waveforms.
Thyristor Converters: Inverter Mode

- Family of curves at various values of delay angle

Figure 6-16  (a) Thyristor inverter with a dc voltage source. (b) $V_d$ versus $I_d$. 

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Thyristor Converters: Inverter Mode

Figure 6-17  Voltage across a thyristor in the inverter mode.

• Importance of extinction angle in inverter mode
Figure 6-18 Waveforms at inverter start-up.

- Waveforms at start-up
3-Phase Thyristor Converters

- Two groups of three thyristors each

Figure 6-19 Three-phase thyristor converter with $L_s = 0$ and a constant dc current.
3-Phase Thyristor Converter Waveforms

- Zero ac-side inductance; purely dc current

Figure 6-20  Waveforms in the converter of Fig. 6-19.
DC-side voltage waveforms assuming zero ac-side inductance
Input Line-Current Waveform

Figure 6-22  Line current in a three-phase thyristor converter of Fig. 6-19.

- Zero ac-side inductance
Input line-current waveforms assuming zero ac-side inductance

Figure 6-23 Line current as a function of $\alpha$. (With permission from ref. 2.)
Three-Phase Thyristor Converter

Figure 6-24 Three-phase converter with $L_s$ and a constant dc current.

- AC-side inductance is included
Current Commutation Waveforms

- Constant dc-side current

Figure 6-25 Commutation in the presence of $L_s$. 
Input Line-Current Waveform

Figure 6-26  Line current in the presence of $L_s$.

- Finite ac-side inductance
Input Line-Current Harmonics

- Finite ac-side inductance

Figure 6-27  Normalized harmonic currents in the presence of $L_r$. (With permission from ref. 2).
Input Line-Current Harmonics

• Typical and idealized

<table>
<thead>
<tr>
<th>Table 6-1 Typical and Idealized Harmonics</th>
</tr>
</thead>
<tbody>
<tr>
<td>h</td>
</tr>
<tr>
<td>-------</td>
</tr>
<tr>
<td>Typical</td>
</tr>
<tr>
<td>Idealized</td>
</tr>
</tbody>
</table>
Three-Phase Thyristor Converter

- Realistic load

Figure 6-28 A practical thyristor converter.
Thyristor Converter Waveforms

Figure 6-29  Waveforms in the converter of Fig. 6-28.

- Realistic load; continuous-conduction mode
Thyristor Converter Waveforms

Figure 6-30  Waveforms in a discontinuous-current-conduction mode.

- Realistic load; discontinuous-conduction mode
Thyristor Inverter

- Constant dc current

Figure 6-31  Inverter with a constant dc current.
Thyristor Inverter Waveforms

- Finite ac-side inductance

Figure 6-32  Waveforms in the inverter of Fig. 6-31.
Thyristor Inverter

- Family of curves at various values of delay angle

Figure 6-33  (a) Thyristor inverter with a dc voltage source.  
(b) $V_d$ versus $I_d$. 

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Chapter 6 Thyristor Converters
Thyristor Inverter Operation

- Importance of extinction angle

Figure 6-34 Voltage across a thyristor in the inverter mode.
Thyristor Converters: Voltage Notching

- Importance of external ac-side inductance

Figure 6-35  Line notching in other equipment voltage: (a) circuit, (b) phase voltages, (c) line-to-line voltage $v_{AB}$. 
Limits on Notching and Distortion

Table 6-2 Line Notching and Distortion Limits for 460-V Systems

<table>
<thead>
<tr>
<th>Class</th>
<th>Line Notch Depth $\rho$ (%)</th>
<th>Line Notch Area $(V \cdot \mu s)$</th>
<th>Voltage Total Harmonic Distortion (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Special applications</td>
<td>10</td>
<td>16,400</td>
<td>3</td>
</tr>
<tr>
<td>General system</td>
<td>20</td>
<td>22,800</td>
<td>5</td>
</tr>
<tr>
<td>Dedicated system</td>
<td>50</td>
<td>36,500</td>
<td>10</td>
</tr>
</tbody>
</table>

- Guidelines
Thyristor Converter Representation

![Diagram of Thyristor Converter Representation]

**Figure 6-36** Summary of thyristor converter output voltage with a dc current $I_d$.

- Functional block diagram

Single-phase full-bridge: $K_1 = 0.9, K_2 = 2$
Three-phase full-bridge: $K_1 = 1.35, K_2 = 3$
Chapter 7

DC-DC Switch-Mode Converters

• dc-dc converters for switch-mode dc power supplies and dc-motor drives
Figure 7-1 A dc–dc converter system.

• Functional block diagram
Stepping Down a DC Voltage

Figure 7-2  Switch-mode dc–dc conversion.

• A simple approach that shows the evolution
Pulse-Width Modulation in DC-DC Converters

• Role of PWM

Figure 7-3 Pulse-width modulator: (a) block diagram; (b) comparator signals.
Step-Down DC-DC Converter

- Pulsating input to the low-pass filter
Step-Down DC-DC Converter: Waveforms

Figure 7-5  Step-down converter circuit states (assuming \( i_L \) flows continuously): (a) switch on; (b) switch off.

- Steady state; inductor current flows continuously
Step-Down DC-DC Converter: Waveforms at the boundary of Cont./Discont. Conduction

Figure 7-6  Current at the boundary of continuous—discontinuous conduction: (a) current waveform; (b) $I_{LB}$ versus $D$ keeping $V_d$ constant.

- Critical current below which inductor current becomes discontinuous
Step-Down DC-DC Converter: Discontinuous Conduction Mode

Figure 7-7 Discontinuous conduction in step-down converter.

- Steady state; inductor current discontinuous

Copyright © 2003 by John Wiley & Sons, Inc. Chapter 7 DC-DC Switch-Mode Converters
Step-Down DC-DC Converter: Limits of Cont./Discont. Conduction

- The duty-ratio of 0.5 has the highest value of the critical current

Figure 7-8  Step-down converter characteristics keeping $V_d$ constant.

$\frac{I_o}{I_{LB, max}} = \frac{T_s V_d}{\delta L}$

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Step-Down DC-DC Converter: Limits of Cont./Discont. Conduction

- Output voltage is kept constant

Figure 7-9 Step-down converter characteristics keeping $V_o$ constant.

$\frac{I_o}{I_{LB,\text{max}}} = \frac{T \cdot V_o}{2L}$
Step-Down Conv.: Output Voltage Ripple

Figure 7-10  Output voltage ripple in a step-down converter.

- ESR is assumed to be zero
Step-Up DC-DC Converter

- Output voltage must be greater than the input
Step-Up DC-DC Converter Waveforms

- Continuous current conduction mode

Figure 7-12  Continuous-conduction mode: (a) switch on; (b) switch off.
Step-Up DC-DC Converter: Limits of Cont./Discont. Conduction

The output voltage is held constant

Figure 7-13  Step-up dc–dc converter at the boundary of continuous–discontinuous conduction.
Step-Up DC-DC Converter: Discont. Conduction

- Occurs at light loads

Figure 7-14 Step-up converter waveforms: (a) at the boundary of continuous—discontinuous conduction; (b) at discontinuous conduction.
Step-Up DC-DC Converter: Limits of Cont./Discont. Conduction

• The output voltage is held constant

**Figure 7-15** Step-up converter characteristics keeping $V_o$ constant.
Step-Up DC-DC Converter: Effect of Parasitics

The duty-ratio is generally limited before the parasitic effects become significant.

Figure 7-16 Effect of parasitic elements on voltage conversion ratio (step-up converter).
Step-Up DC-DC Converter Output Ripple

Figure 7-17  Step-up converter output voltage ripple.

• ESR is assumed to be zero
Step-Down/Up DC-DC Converter

- The output voltage can be higher or lower than the input voltage.

**Figure 7-18** Buck-boost converter.
Step-Up DC-DC Converter: Waveforms

- Continuation conduction mode

Figure 7-19 Buck-boost converter ($i_L > 0$): (a) switch on; (b) switch off.
Step-Up DC-DC Converter: Limits of Cont./Discont. Conduction

- The output voltage is held constant

Figure 7-20 Buck–boost converter: boundary of continuous—discontinuous conduction.
Step-Up DC-DC Converter: Discontinuous Conduction Mode

Figure 7-21 Buck-boost converter waveforms in a discontinuous-conduction mode.

- This occurs at light loads
Step-Up DC-DC Converter: Limits of Cont./Discont. Conduction

- The output voltage is held constant
Step-Up DC-DC Converter: Effect of Parasitics

- The duty-ratio is limited to avoid these parasitic effects from becoming significant

![Diagram showing the effect of parasitic elements on the voltage conversion ratio in a buck-boost converter.](image)
Step-Up DC-DC Converter: Output Voltage Ripple

- ESR is assumed to be zero

Figure 7-24 Output voltage ripple in a buck-boost converter.
Cuk DC-DC Converter

- The output voltage can be higher or lower than the input voltage
Cuk DC-DC Converter: Waveforms

- The capacitor voltage is assumed constant

Figure 7-26  Cuk converter waveforms: (a) switch off; (b) switch on.
Converter for DC-Motor Drives

- Four quadrant operation is possible

Figure 7-27 Full-bridge dc–dc converter.
Converter Waveforms

- Bi-polar voltage switching
Converter Waveforms

- Uni-polar voltage switching
Output Ripple in Converters for DC-Motor Drives

### Figure 7-30

$V_{r, \text{rms}}$ in a full-bridge converter using PWM:
(a) with bipolar voltage switching; (b) with unipolar voltage switching.

- bi-polar and uni-polar voltage switching
Switch Utilization in DC-DC Converters

- It varies significantly in various converters.

Figure 7-31 Switch utilization in dc–dc converters.
Equivalent Circuits in DC-DC Converters

- replacing inductors and capacitors by current and voltage sources, respectively

Figure 7-32  Converter equivalent circuits: (a) step-down; (b) step-up; (c) step-down/step-up; (d) Ćuk; (e) full-bridge.
Reversing the Power Flow in DC-DC Conv.

• For power flow from right to left, the input current direction should also reverse.

Figure 7-33 Reversible power flow with reversible direction of the output current $i_o$. 

For power flow from right to left, the input current direction should also reverse.
• converters for ac motor drives and uninterruptible power supplies
Switch-Mode DC-AC Inverter

![Diagram of a switch-mode DC-AC inverter](image)

**Figure 8-1** Switch-mode inverter in ac motor drive.

- Block diagram of a motor drive where the power flow is unidirectional.
Switch-Mode DC-AC Inverter

Figure 8-2 Switch-mode converters for motoring and regenerative braking in ac motor drive.

- Block diagram of a motor drive where the power flow can be bi-directional
Switch-Mode DC-AC Inverter

- Four quadrants of operation

**Figure 8-3** Single-phase switch-mode inverter.
One Leg of a Switch-Mode DC-AC Inverter

- The mid-point shown is fictitious
Synthesis of a Sinusoidal Output by PWM

Figure 8-5  Pulse-width modulation.
Details of a Switching Time Period

Figure 8-6 Sinusoidal PWM.

- Control voltage can be assumed constant during a switching time-period
Harmonics in the DC-AC Inverter Output Voltage

<table>
<thead>
<tr>
<th>Table 8-1</th>
<th>Generalized Harmonics of $v_{Ao}$ for a Large $m_f$.</th>
</tr>
</thead>
<tbody>
<tr>
<td>$h$</td>
<td>$0.2$</td>
</tr>
<tr>
<td>$m_a$</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>$m_f$</td>
</tr>
<tr>
<td></td>
<td>1.242</td>
</tr>
<tr>
<td></td>
<td>$m_f \pm 2$</td>
</tr>
<tr>
<td></td>
<td>$m_f \pm 4$</td>
</tr>
<tr>
<td>2$m_f \pm 1$</td>
<td>0.190</td>
</tr>
<tr>
<td>2$m_f \pm 3$</td>
<td></td>
</tr>
<tr>
<td>2$m_f \pm 5$</td>
<td></td>
</tr>
<tr>
<td>3$m_f$</td>
<td></td>
</tr>
<tr>
<td>3$m_f \pm 2$</td>
<td>0.044</td>
</tr>
<tr>
<td>3$m_f \pm 4$</td>
<td></td>
</tr>
<tr>
<td>3$m_f \pm 6$</td>
<td></td>
</tr>
<tr>
<td>4$m_f \pm 1$</td>
<td>0.163</td>
</tr>
<tr>
<td>4$m_f \pm 3$</td>
<td></td>
</tr>
<tr>
<td>4$m_f \pm 5$</td>
<td></td>
</tr>
<tr>
<td>4$m_f \pm 7$</td>
<td></td>
</tr>
</tbody>
</table>

Note: $(\bar{V}_{Ao})_{h/2}V_d = (\bar{V}_{AN})_{h/2}V_d$ is tabulated as a function of $m_a$.

- Harmonics appear around the carrier frequency and its multiples
Harmonics due to Over-modulation

Figure 8-7  Harmonics due to overmodulation; drawn for $m_a = 2.5$ and $m_f = 15$.

- These are harmonics of the fundamental frequency
Output voltage Fundamental as a Function of the Modulation Index

- Shows the linear and the over-modulation regions; square-wave operation in the limit

Figure 8-8  Voltage control by varying $m_a$. 

$\frac{V_{Ao}}{V_d}$

$\frac{4}{\pi} (= 1.278)$

1.0

Linear

over-modulation

Square-wave

$0 \rightarrow 1.0 \rightarrow 3.24$ (for $m_f = 15$)
Square-Wave Mode of Operation

- Harmonics are of the fundamental frequency

Figure 8-9  Square-wave switching.
Half-Bridge Inverter

- Capacitors provide the mid-point

Figure 8-10  Half-bridge inverter.
Single-Phase Full-Bridge DC-AC Inverter

Figure 8-11  Single-phase full-bridge inverter.

- Consists of two inverter legs
PWM to Synthesize Sinusoidal Output

- The dotted curve is the desired output; also the fundamental frequency.

Figure 8-12  PWM with bipolar voltage switching.
Analysis assuming Fictitious Filters

- Small fictitious filters eliminate the switching-frequency related ripple

**Figure 8-13** Inverter with "fictitious" filters.
DC-Side Current

\[ v_o \]

\[ v_o \text{(filtered)} \]

\[ V_d \]

\[ \omega_1 t \]

\[ i_d \]

\[ i_o \]

\[ i_d2 \]

\[ 0 \]

\[ \phi \]

\[ I_d \]

\[ \omega_1 t \]

**Figure 8-14** The dc-side current in a single-phase inverter with PWM bipolar voltage switching.

- Bi-Polar Voltage switching
Output Waveforms: Uni-polar Voltage Switching

- Harmonic components around the switching frequency are absent

Figure 8-15  PWM with unipolar voltage switching (single phase).
DC-Side Current in a Single-Phase Inverter

Figure 8-16  The dc-side current in a single-phase inverter with PWM unipolar voltage switching.

- Uni-polar voltage switching
Sinusoidal Synthesis by Voltage Shift

- Phase shift allows voltage cancellation to synthesize a 1-Phase sinusoidal output

Figure 8-17  Full-bridge, single-phase inverter control by voltage cancellation: (a) power circuit; (b) waveforms; (c) normalized fundamental and harmonic voltage output and total harmonic distortion as a function of $\alpha$. 

$\beta = \frac{(180 - \alpha)^2}{2} = \frac{90 - \frac{\alpha}{2}}{2}$
Single-Phase Inverter

Figure 8-18  Single-phase inverter: (a) circuit; (b) fundamental-frequency components; (c) ripple frequency components; (d) fundamental-frequency phasor diagram.

• Analysis at the fundamental frequency
Square-Wave and PWM Operation

- PWM results in much smaller ripple current

Figure 8-19  Ripple in the inverter output: (a) square-wave switching; (b) PWM bipolar voltage switching.
Push-Pull Inverter

- Low Voltage to higher output using square-wave operation

Figure 8-20 Push–pull inverter (single phase).
Three-Phase Inverter

Figure 8-21 Three-phase inverter.

- Three inverter legs; capacitor mid-point is fictitious
Three-Phase PWM Waveforms

Figure 8-22 Three-phase PWM waveforms and harmonic spectrum.
Three-Phase Inverter Harmonics

Table 8-2 Generalized Harmonics of $v_{ll}$ for a Large and Odd $m_f$ That Is a Multiple of 3.

<table>
<thead>
<tr>
<th>$h$</th>
<th>$m_a$</th>
<th>0.2</th>
<th>0.4</th>
<th>0.6</th>
<th>0.8</th>
<th>1.0</th>
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<tbody>
<tr>
<td>1</td>
<td></td>
<td>0.122</td>
<td>0.245</td>
<td>0.367</td>
<td>0.490</td>
<td>0.612</td>
</tr>
<tr>
<td>$m_f \pm 2$</td>
<td></td>
<td>0.010</td>
<td>0.037</td>
<td>0.080</td>
<td>0.135</td>
<td>0.195</td>
</tr>
<tr>
<td>$m_f \pm 4$</td>
<td></td>
<td></td>
<td>0.005</td>
<td>0.011</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$2m_f \pm 1$</td>
<td></td>
<td>0.116</td>
<td>0.200</td>
<td>0.227</td>
<td>0.192</td>
<td>0.111</td>
</tr>
<tr>
<td>$2m_f \pm 5$</td>
<td></td>
<td></td>
<td></td>
<td>0.008</td>
<td>0.020</td>
<td></td>
</tr>
<tr>
<td>$3m_f \pm 2$</td>
<td></td>
<td>0.027</td>
<td>0.085</td>
<td>0.124</td>
<td>0.108</td>
<td>0.038</td>
</tr>
<tr>
<td>$3m_f \pm 4$</td>
<td></td>
<td></td>
<td></td>
<td>0.007</td>
<td>0.029</td>
<td>0.064</td>
</tr>
<tr>
<td>$4m_f \pm 1$</td>
<td></td>
<td>0.100</td>
<td>0.096</td>
<td>0.005</td>
<td>0.064</td>
<td>0.042</td>
</tr>
<tr>
<td>$4m_f \pm 5$</td>
<td></td>
<td></td>
<td></td>
<td>0.021</td>
<td>0.051</td>
<td>0.073</td>
</tr>
<tr>
<td>$4m_f \pm 7$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.010</td>
<td>0.030</td>
</tr>
</tbody>
</table>

Note: $(V_{ll})_h/V_d$ are tabulated as a function of $m_a$ where $(V_{ll})_h$ are the rms values of the harmonic voltages.
Three-Phase Inverter Output

\[ \frac{V_{LL_1}}{V_d} \]

\[ \frac{\sqrt{6}}{\pi} = 0.78 \]

\[ \frac{\sqrt{3}}{2\sqrt{2}} = 0.612 \]

(for \( m_f = 15 \))

**Figure 8-23** Three-phase inverter; \( V_{LL_1}(\text{rms})/V_d \) as a function of \( m_a \).

- Linear and over-modulation ranges
Three-Phase Inverter: Square-Wave Mode

- Harmonics are of the fundamental frequency

Figure 8-24  Square-wave inverter (three phase).
Three-Phase Inverter: Fundamental Frequency

• Analysis at the fundamental frequency can be done using phasors

Figure 8-25  Three-phase inverter: (a) circuit diagram; (b) phasor diagram (fundamental frequency).

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Square-Wave and PWM Operation

- PWM results in much smaller ripple current

Figure 8-26 Phase-to-load-neutral variables of a three-phase inverter: (a) square wave; (b) PWM.
DC-Side Current in a Three-Phase Inverter

Figure 8-27  Input dc current in a three-phase inverter.

- The current consists of a dc component and the switching-frequency related harmonics
Square-Wave Operation

Figure 8-28 Square-wave inverter: phase A waveforms.

- devices conducting are indicated
PWM Operation

• devices conducting are indicated

Figure 8-29  PWM inverter waveforms: load power factor angle = 30° (lag).
Short-Circuit States in PWM Operation

Figure 8-30 Short-circuit states in a three-phase PWM inverter.

- top group or the bottom group results in short circuiting three terminals
Effect of Blanking Time

- Results in nonlinearity
Effect of Blanking Time

- Voltage jump when the current reverses direction

Figure 8-32  Effect of $t_\Delta$ on $V_o$, where $\Delta V_o$ is defined as a voltage drop if positive.
Effect of Blanking Time

- Effect on the output voltage

Figure 8-33 Effect of $t_{\Delta}$ on the sinusoidal output.
Programmed Harmonic Elimination

- Angles based on the desired output

Figure 8-34  Programmed harmonic elimination of fifth and seventh harmonics.
Tolerance-Band Current Control

Figure 8-35  Tolerance band current control.

- Results in a variable frequency operation
Fixed-Frequency Operation

- Better control is possible using $dq$ analysis

**Figure 8-36** Fixed-frequency current control.
Transition from Inverter to Rectifier Mode

- Can analyze based on the fundamental-frequency components

Figure 8-37  Operation modes: (a) circuit; (b) inverter mode; (c) rectifier mode; (d) constant $I_A$. 
Summary of DC-AC Inverters

• Functional representation in a block-diagram form

![Block diagram of DC-AC inverters](image)

\[ V_d \rightarrow k(m_a) \rightarrow V_{o1} = k(m_a) V_d \] (rms, line-line)

\[ V_d \rightarrow \text{Inverter} \rightarrow V_{o1} = k V_d \] (rms, line-to-line)

- for \( m_a \leq 1.0 \)
  - \( k(m_a) = 0.707 m_a \) 1-phase
  - \( k(m_a) = 0.612 m_a \) 3-phase

\( (a) \)

- \( k = 0.9 \) 1-phase
- \( k = 0.78 \) 3-phase

\( (b) \)

**Figure 8-38** Summary of inverter output voltages: (a) PWM operation \((m_a \leq 1)\); (b) square-wave operation.
Chapter 9

Zero-Voltage or Zero-Current Switchings

- converters for soft switching
One Inverter Leg

- The output current can be positive or negative

Figure 9-1 One inverter leg.
Hard Switching Waveforms

- The output current can be positive or negative.

**Figure 9-2** Switch-mode inductive current switchings.

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Turn-on and Turn-off Snubbers

- Turn-off snubbers are used

Figure 9-3 Dissipative snubbers: (a) snubber circuits; (b) switching loci with snubbers.
Switching Trajectories

• Comparison of Hard versus soft switching

Figure 9-4  Zero-voltage-/zero-current-switching loci.
Undamped Series-Resonant Circuit

Figure 9-5 Undamped series-resonant circuit; $i_L$ and $v_c$ are normalized: (a) circuit; (b) waveforms with $I_{LO} = 0.5, V_{c0} = 0.75$.

- The waveforms shown include initial conditions
Series-Resonant Circuit with Capacitor-Parallel Load

- The waveforms shown include initial conditions

*Figure 9-6* Series-resonant circuit with capacitor-parallel load \( (i_L \text{ and } v_c \text{ are normalized}) \):

(a) circuit; (b) \( V_{in} = 0 \), \( I_{L0} = I_o = 0.5 \).
The impedance is capacitive below the resonance frequency.
Undamped Parallel-Resonant Circuit

- Excited by a current source

Figure 9-8 Undamped parallel-resonant circuit.
Impedance of a Parallel-Resonant Circuit

- The impedance is inductive at below the resonant frequency
Series Load Resonant (SLR) Converter

- The transformer is ignored in this equivalent circuit.

Figure 9-10  SLR dc–dc converter: (a) half-bridge; (b) equivalent circuit.
SLR Converter Waveforms

Figure 9-11  SLR dc–dc converter; discontinuous-conduction mode with $\omega_s < \frac{1}{2} \omega_0$.

- The operating frequency is below one-half the resonance frequency
The operating frequency is in between one-half the resonance frequency and the resonance frequency.
SLR Converter Waveforms

- The operating frequency is above the resonance frequency

Figure 9-13  SLR dc–dc converter; continuous-conduction mode with $\omega_s > \omega_0$. 

Copyright © 2003 by John Wiley & Sons, Inc. Chapter 9 Resonant Converters 9-14
Lossless Snubbers in SLR Converters

- The operating frequency is above the resonance frequency

Figure 9-14. Lossless snubbers in an SLR converter at $\omega_s > \omega_0$. 

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SLR Converter Characteristics

- Output Current as a function of operating frequency for various values of the output voltage

Figure 9-15 Steady-state characteristics of an SLR dc–dc converter; all parameters are normalized.
SLR Converter Control

- The operating frequency is varied to regulate the output voltage

Figure 9-16  Control of SLR dc–dc converter.
Parallel Load Resonant (PLR) Converter

Figure 9-17  PLR dc–dc converter: (a) half-bridge; (b) equivalent circuit.

- The transformer is ignored in this equivalent circuit
PLR Converter Waveforms

- The current is in a discontinuous conduction mode

Figure 9-18 PLR dc–dc converter in a discontinuous mode.
PLR Converter Waveforms

Figure 9-19  PLR dc–dc converter in a continuous mode with $\omega_s < \omega_0$.

- The operating frequency is below the resonance frequency
PLR Converter Waveforms

Figure 9-20  PLR dc–dc converter in a continuous mode with \( \omega_s > \omega_0 \).

- The operating frequency is above the resonance frequency
PLR Converter Characteristics

Figure 9-21 Steady-state characteristics of a PLR dc–dc converter. All quantities are normalized.

- Output voltage as a function of operating frequency for various values of the output current
Hybrid-Resonant DC-DC Converter

- Combination of series and parallel resonance

Figure 9-22 Hybrid-resonant dc–dc converter.
Parallel-Resonant Current-Source Converter

Figure 9-23 Basic circuit for current-source, parallel-resonant converter for induction heating: (a) basic circuit; (b) phasor diagram at $\omega_s = \omega_0$; (c) phasor diagram at $\omega_s > \omega_0$.

- Basic circuit to illustrate the operating principle at the fundamental frequency
Parallel-Resonant Current-Source Converter

Figure 9-24  Current-source, parallel-resonant inverter for induction heating: (a) circuit; (b) waveforms.

- Using thyristors; for induction heating
Class-E Converters

Figure 9-25  Class E converter (optimum mode, $D = 0.5$).
Class-E Converters

![Class-E Converter Diagram](image)

Figure 9-26 Class E converter (nonoptimum mode).

Non-Optimum mode
Resonant Switch Converters

Classifications

Figure 9-27  Resonant-switch converters: (a) ZCS dc–dc converter (step-down); (b) ZVS dc–dc converter (step-down); (c) ZVS-CV dc–dc converter (step-down).
ZCS Resonant-Switch Converter

Figure 9-28  ZCS resonant-switch dc–dc converter.

• One possible implementation
ZCS Resonant-Switch Converter

Figure 9-29 $v_{oi}$ waveform in a ZCS resonant-switch dc–dc converter.

- Waveforms; voltage is regulated by varying the switching frequency
ZCS Resonant-Switch Converter

- A practical circuit

Figure 9-30 ZCS resonant-switch dc–dc converter; alternate configuration.
ZVS Resonant-Switch Converter

- Serious limitations

Figure 9-31  ZVS resonant-switch dc–dc converter.
ZVS Resonant-Switch Converter

Figure 9-32  The $v_{oi}$ waveform in a ZVS resonant-switch dc–dc converter.

- Waveforms
MOSFET Internal Capacitances

- These capacitances affect the MOSFET switching

Figure 9-33  Switch internal capacitances.
**ZVS-CV DC-DC Converter**

- The inductor current must reverse direction during each switching cycle.

**Figure 9-34** ZVS-CV dc–dc converter.
ZVS-CV DC-DC Converter

- One transition is shown

Figure 9-35  ZVS-CV dc–dc converter; $T_+$, $T_-$ off.
ZVS-CV Principle Applied to DC-AC Inverters

- Very large ripple in the output current

Figure 9-36 ZVS-CV dc-to-ac inverter: (a) half-bridge; (b) square-wave mode; (c) current-regulated mode.
Three-Phase ZVS-CV DC-AC Inverter

Figure 9-37  Three-phase, ZVS-CV dc-to-ac inverter.

- Very large ripple in the output current
Output Regulation by Voltage Control

- Each pole operates at nearly 50% duty-ratio

Figure 9-38 Voltage control by voltage cancellation: conventional switch-mode converter.
ZVS-CV with Voltage Cancellation

- Commonly used
• The dc-link voltage is made to oscillate

Figure 9-40  Resonant-dc-link inverter, basic concept: (a) basic circuit; (b) lossless $R_f = 0$; (c) losses are present.
Three-Phase Resonant DC-Link Inverter

Figure 9-41 Three-phase resonant-dc-link inverter.

• Modifications have been proposed
High-Frequency-Link Inverter

• Basic principle for selecting integral half-cycles of the high-frequency ac input

Figure 9-42 High-frequency-link integral-half-cycle inverter.
High-Frequency-Link Inverter

Figure 9-43  Synthesis of low-frequency ac output.

- Low-frequency ac output is synthesized by selecting integral half-cycles of the high-frequency ac input
High-Frequency-Link Inverter

Figure 9-44  High-frequency ac to low-frequency three-phase ac converter.

• Shows how to implement such an inverter
• One of the most important applications of power electronics
Linear Power Supplies

- Very poor efficiency and large weight and size

Figure 10-1  Linear power supply: (a) schematic; (b) selection of transformer turns ratio so that $V_{d,\text{min}} > V_o$ by a small margin.
Switching DC Power Supply: Block Diagram

- High efficiency and small weight and size

Figure 10-2 Schematic of a switch-mode dc power supply.
Switching DC Power Supply: Multiple Outputs

- In most applications, several dc voltages are required, possibly electrically isolated from each other.
Transformer Analysis

- Needed to discuss high-frequency isolated supplies
PWM to Regulate Output

- Basic principle is the same as discussed in Chapter 8

Figure 10-5  PWM Scheme used in dc–dc converters, where the converter output is rectified to produce a dc output.

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Chapter 10 Switching
DC Power Supplies
Flyback Converter

- Derived from buck-boost; very power at small power (> 50 W) power levels

Figure 10-6  Flyback converter.
Figure 10-7  Flyback converter circuit states: (a) switch on; (b) switch off.

- Switch on and off states (assuming incomplete core demagnetization)
Flyback Converter

Figure 10-8  Flyback converter waveforms.

- Switching waveforms (assuming incomplete core demagnetization)
Other Flyback Converter Topologies

- Not commonly used

**Figure 10-9** Other flyback topologies: (a) two-transistor flyback converter; (b) paralleled flyback converters.
Forward Converter

![Forward Converter Circuit Diagram]

Figure 10-10  Idealized forward converter.

- Derived from Buck; idealized to assume that the transformer is ideal (not possible in practice)
Forward Converter: in Practice

- Switching waveforms (assuming incomplete core demagnetization)
Forward Converter: Other Possible Topologies

Two-switch Forward converter is very commonly used.
Push-Pull Inverter

- Leakage inductances become a problem

Figure 10-13  Push-pull converter.
Half-Bridge Converter

- Derived from Buck

Figure 10-14  Half-bridge dc–dc converter.
Full-Bridge Converter

- Used at higher power levels (> 0.5 kW)

Figure 10-15 Full-bridge converter.
Current-Source Converter

Figure 10-16  Current source converter \((D > 0.5)\).

- More rugged (no shoot-through) but both switches must not be open simultaneously
Ferrite Core Material

- Several materials to choose from based on applications

Figure 10-17  3C8 ferrite characteristic curves: (a) B–H loop; (b) core loss curves. (Courtesy of Ferroxcube Division of Amperex Electronic Corporation.)
Core Utilization in Various Converter Topologies

• At high switching frequencies, core losses limit excursion of flux density

Figure 10-18  Core excitation: (a) forward converter, $D = 0.5$; (b) full-bridge converter, $D = 0.5$. 

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Control to Regulate Voltage Output

- Linearized representation of the feedback control system.

Figure 10-19 Voltage regulation: (a) feedback control system; (b) linearized feedback control system.
Forward Converter: An Example

- The switch and the diode are assumed to be ideal

Figure 10-20  Forward converter: (a) circuit; (b) switch on; (c) switch off.

\[
\begin{align*}
V_d &= 8 \text{ V} \\
V_o &= 5 \text{ V} \\
r_L &= 20 \text{ m\Omega} \\
L &= 5 \mu\text{H} \\
r_c &= 10 \text{ m\Omega} \\
C &= 2,000 \mu\text{F} \\
R &= 200 \text{ m\Omega} \\
f_s &= 200 \text{ kHz}
\end{align*}
\]
Forward Converter: Transfer Function Plots

- Example considered earlier.

Figure 10.21 (a) Gain plot of the forward converter in Fig. 10.20a.
(b) Phase plot of the forward converter in Fig. 10.20a.
Flyback Converter: Transfer Function Plots

- An example

![Flyback Converter Transfer Function Plots](image)

Figure 10-22  (a) Gain plot for a flyback converter. (b) Phase plot for a flyback converter.
Linearizing the PWM Block

Figure 10-23  Pulse-width modulator.

- The transfer function is essentially a constant with zero phase shift
Gain of the PWM IC

- It is slope of the characteristic

**Figure 10-24** Pulse-width modulator transfer function.
Typical Gain and Phase Plots of the Open-Loop Transfer Function

\[ \text{Gain} = 20 \log |T_{OL}(j\omega)| \]

\[ \text{Phase} \phi_{OL} \text{ in degrees} \]

- Definitions of the crossover frequency, phase and gain margins

**Figure 10-25** Gain and phase margins.
A General Amplifier for Error Compensation

\[ v_o = V_o + \tilde{v}_o \]

The converter output (in Fig. 8-19a)

\[ V_o, \text{ ref} \]

Control voltage \( v_c = V_c + \tilde{v}_c \)

**Figure 10-26** A general compensated error amplifier.

- Can be implemented using a single op-amp
Type-2 Error Amplifier

\[ G_c \]

\[ \psi_c \]

\[ \phi \]

\[ \omega_c \]

\[ \omega_p \]

\[ \sqrt{\omega_c \omega_p} = \omega_{cross} \] (log scale)

\[ v_o \]

\[ v_c \]

(a)

Figure 10-27  Error amplifier.

- Shows phase boost at the crossover frequency
Voltage Feed-Forward

- Makes converter immune from input voltage variations

Figure 10-28  Voltage feed-forward: effect on duty ratio.
Voltage versus Current Mode Control

- Regulating the output voltage is the objective in both modes of control.
Various Types of Current Mode Control

- Constant frequency, peak-current mode control is used most frequently.

Figure 10-30 Three types of current-mode control: (a) tolerance band control; (b) constant-off-time control; (c) constant frequency with turn-on at clock time.
Peak Current Mode Control

![Graph showing Peak Current Mode Control]

Figure 10-31 Slope compensation in current-mode control ($D_2$ is smaller for a higher input voltage with a constant $V_o$).

- Slope compensation is needed
A Typical PWM Control IC

- Many safety control functions are built in
Current Limiting

Figure 10-33  Current limiting: (a) constant current limiting; (b) foldback current limiting.

- Two options are shown
Implementing Electrical Isolation in the Feedback Loop

- Two ways are shown
Implementing Electrical Isolation in the Feedback Loop

• A dedicated IC for this application is available

Figure 10-35  Isolated feedback generator UC1901. (Courtesy of Unitrode Integrated Circuits Corp.)
Input Filter

- Needed to comply with the EMI and harmonic limits

**Figure 10-36** Input filter.
ESR of the Output Capacitor

- ESR often dictates the peak-peak voltage ripple

Figure 10-37  ESR in the output capacitor.
Chapter 11
Power Conditioners and Uninterruptible Power Supplies

Chapter 11  Power Conditioners and Uninterruptible Power Supplies

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11-2 Power Line Disturbances  354  
11-3 Power Conditioners  357  
11-4 Uninterruptible Power Supplies (UPSs)  358

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• Becoming more of a concern as utility de-regulation proceeds
Distortion in the Input Voltage

- The voltage supplied by the utility may not be sinusoidal.

Figure 11-1 Possible distortions in input voltage: (a) chopped voltage waveform; (b) distorted voltage waveform due to harmonics.
Typical Voltage Tolerance Envelope for Computer Systems

- This has been superceded by a more recent standard

Figure 11-2  Typical computer system voltage tolerance envelope. (Source: IEEE Std. 446, "Recommended Practice for Emergency and Standby Power Systems for Industrial and Commercial Applications.")


## Typical Range of Input Power Quality

### Table 11-1 Typical Range of Input Power Quality and Load Parameters of Major Computer Manufacturers

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Range or Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Voltage regulation, steady state</td>
<td>+5, −10 to +10%, −15% (ANSI C84.1—1970 is +6, −13%)</td>
</tr>
<tr>
<td>2. Voltage disturbances</td>
<td></td>
</tr>
<tr>
<td>a. Momentary undervoltage</td>
<td>−25 to −30% for less than 0.5 s, with −100% acceptable for 4–20 ms</td>
</tr>
<tr>
<td>b. Transient overvoltage</td>
<td>+150 to 200% for less than 0.2 ms</td>
</tr>
<tr>
<td>3. Voltage harmonic distortion(^b)</td>
<td>3–5% (with linear load)</td>
</tr>
<tr>
<td>4. Noise</td>
<td>No standard</td>
</tr>
<tr>
<td>5. Frequency variation</td>
<td>60 Hz ± 0.5 Hz to ±1 Hz</td>
</tr>
<tr>
<td>6. Frequency rate of change</td>
<td>1 Hz/s (slew rate)</td>
</tr>
<tr>
<td>7. 3φ, Phase voltage unbalance(^c)</td>
<td>2.5–5%</td>
</tr>
<tr>
<td>8. 3φ, Load unbalance(^d)</td>
<td>5–20% maximum for any one phase</td>
</tr>
<tr>
<td>9. Power factor</td>
<td>0.8–0.9</td>
</tr>
<tr>
<td>10. Load demand</td>
<td>0.75–0.85 (of connected load)</td>
</tr>
</tbody>
</table>

\(^a\)Parameters 1, 2, 5, and 6 depend on the power source, while parameters 3, 4, and 7 are the product of an interaction of source and load, and parameters 8, 9, and 10 depend on the computer load alone.

\(^b\)Computed as the sum of all harmonic voltages added vectorially.

\(^c\)Computed as follows:

\[
\text{Percent phase voltage unbalance} = \frac{3(V_{\text{max}} - V_{\text{min}})}{V_a + V_b + V_c} \times 100
\]

\(^d\)Computed as difference from average single-phase load.

Source: IEEE Std. 446, "Recommended Practice for Emergency and Standby Power Systems for Industrial and Commercial Applications."
Electronic Tap Changers

- Controls voltage magnitude by connecting the output to the appropriate transformer tap

Figure 11-3  Electronic tap changer.
Uninterruptible Power Supplies (UPS)

Figure 11-4 A UPS block diagram.

- Block diagram; energy storage is shown to be in batteries but other means are being investigated.
UPS: Possible Rectifier Arrangements

- The input normally supplies power to the load as well as charges the battery bank.
UPS: Another Possible Rectifier Arrangement

• Consists of a high-frequency isolation transformer

Figure 11-6 Rectifier consisting of a high-frequency isolation transformer.

- Consists of a high-frequency isolation transformer
UPS: Another Possible Input Arrangement

Figure 11-7 A rectifier with a separate battery charger circuit.

- A separate small battery charger circuit
Battery Charging Waveforms as Function of Time

Figure 11-8  Charging of a battery after a line outage causes battery discharge.

- Initially, a discharged battery is charged with a constant current
UPS: Various Inverter Arrangements

- Depends on applications, power ratings

Figure 11-9 Various inverter arrangements.
**Figure 11-10** Uninterruptible power supply control.

- Typically the load is highly nonlinear and the voltage output of the UPS must be as close to the desired sinusoidal reference as possible
• With higher power UPS supplying several loads, malfunction within one load should not disturb the other loads.
Another Possible UPS Arrangement

- Functions of battery charging and the inverter are combined

Figure 11-12 A UPS arrangement where the functions of battery charging and inverter are combined.

- Functions of battery charging and the inverter are combined
UPS: Using the Line Voltage as Backup

- Needs static transfer switches

Figure 11-13 Line as backup.
Chapter 12
Introduction to Motor Drives

• Motor drives are one of the most important applications of power electronics
Control Structure of Drives

**Figure 12-1** Control of motor drives.

- Very general description
Servo Drives

Figure 12-2 Servo drives.

- The basic structure is the same regardless of the drive that is selected.
An Example of Adjustable Speed Drives

**Figure 12-3** Adjustable-speed drive in an air conditioning system.

- The speed of the drive response is not important here
A Representation of the Load on a Drive

Figure 12-4 Load profile: (a) load–motion profile; (b) load–torque profile (assuming a purely inertial load).

- This cycle may repeat continuously
Two Coupling Mechanisms

- Commonly used

Figure 12-5  Coupling mechanisms: (a) gear; (b) feed screw.
Instantaneous Waveforms of Torque and Current

- Their RMS values may determine the limit

*Figure 12-6*  Motor torque and current.
Simplified Circuit of a Drive

- Allows discussion of various parameters and operating conditions on losses and ratings

Figure 12-7  Simplified circuit of a motor drive.
Control of Servo Drives

- The structure is application dependent.

Figure 12-8 Control of servo drives: (a) inner current loop; (b) no inner current loop.
Limiters in the Control Structure

Figure 12-9  Ramp limiter to limit motor current.

- By providing ramp limiters, for example, drive can be prevented from "triping" under sudden changes
• These drives continue to be used
DC-Motor Structure

Figure 13-1  A dc motor: (a) permanent-magnet motor; (b) dc motor with a field winding.

- With permanent magnets or a wound field
DC-Motor Equivalent Circuit

- The mechanical system can also be represented as an electrical circuit.
Four-Quadrant Operation of DC-Motor Drives

Figure 13-3  Four-quadrant operation of a dc motor.

- High performance drives may operate in all four quadrants
DC-Motor Drive Torque-Speed Characteristics and Capabilities

- With permanent magnets

Figure 13-4 Permanent-magnet dc motor: (a) equivalent circuit; (b) torque-speed characteristics: $V_{c1} > V_{c2} > V_{c3} > V_{f1}$, where $V_{c4}$ is the rated voltage; (c) continuous torque-speed capability.
DC-Motor Drive Capabilities

- Separately-Excited field

Figure 13-5  Separately excited dc motor: (a) equivalent circuit; (b) continuous torque-speed capability.
Controlling Torque, Speed and Position

- Cascaded control is commonly used

Figure 13-6 Closed-loop position/speed dc servo drive.
Small-Signal Representation of DC Machines

Figure 13-7 Block diagram representation of the motor and load (without any feedback).

- Around a steady state operating point
Electrical Time-Constant of the DC Machine

Figure 13-8  Electrical time constant $\tau_e$; speed $\omega_m$ is assumed to be constant.

- The speed is assumed constant
Mechanical Time-Constant of the DC Machine

- The load-torque is assumed constant
DC-Motor Drive: Four-Quadrant Capability

If a diode-rectifier is used, the energy recovered during regenerative braking is dissipated in a resistor.

Figure 13-10  A dc motor servo drive; four-quadrant operation.
Ripple in the Armature Current

\[ (\Delta I_{p-p})_{\text{max}} = \frac{V_d}{2L_\alpha f_s} \]

\[ T_s = \frac{1}{f_s} \]

\[ V_t = \frac{V_d}{2} \]

\[ (\Delta I_{p-p})_{\text{max}} = \frac{V_d}{8L_\alpha f_s} \]

Figure 13-11  Ripple \( i_r \) in the armature current: (a) PWM bipolar voltage switching, \( V_t = 0 \); (b) PWM unipolar voltage switching, \( V_t = \frac{1}{2} V_d \).

- Bi-polar and uni-polar voltage switchings
Control of Servo Drives

![Diagram of control of servo drives](image)

*Figure 13-12* Control of servo drives: (a) no internal current-control loop; (b) internal current-control loop.

- A concise coverage is presented in “Electric Drives: An Integrative Approach” by N. Mohan (www.MNPERE.com)
Effect of Blanking Time

Figure 13-13  Effect of blanking time.

- Non-linearity is introduced
Converters for Limited Operational Capabilities

- Two switches for 2-quadrant operation and only one switch for 1-quadrant operation

Figure 13-14  (a) Two-quadrant operation; (b) single-quadrant operation.

- Two switches for 2-quadrant operation and only one switch for 1-quadrant operation
Line-Controlled Converters for DC Drives

Figure 13-15 Line-frequency-controlled converters for dc motor drives: (a) single-phase input; (b) three-phase input.

- Large low-frequency ripple in the dc output of converters
Four Quadrant Operation using Line Converters

- Two options to achieve 4-quadrant operation

Figure 13-16 Line-frequency-controlled converters for four-quadrant operation:
(a) back-to-back converters for four-quadrant operation (without circulating current);
(b) converter operation modes; (c) contactors for four-quadrant operation.
Effect of Discontinuous Current Conduction

- Speed goes up unless it is controlled

Figure 13-17  Effect of discontinuous $i_a$ on $\omega_m$. 

(low values of $I_a$)

$\alpha = \text{constant}$
Open-Loop Speed Control

Figure 13-18  Open-loop speed control.

- Adequate for general-purpose applications
DC Drive Characteristics and Capabilities

- Line current in switch-mode and line-converter drives
Chapter 14
Induction Motor Drives

- Extremely large potential as adjustable speed drives
Pump Application: Adjustable Flow rate

- Fixed versus adjustable speed drive

Figure 14-1  Centrifugal pump: (a) constant-speed drive; (b) adjustable-speed drive.
Per-Phase Representation

**Figure 14-2** Per-phase representation: (a) equivalent circuit; (b) phasor diagram.

- Assuming sinusoidal steady state
## Important Relationships in an Induction Machine

### Table 14-1 Important Relationships

<table>
<thead>
<tr>
<th>Expression</th>
<th>Relationship</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \omega_s = k_7f )</td>
<td>( \omega_s = \omega_r + s \omega_r )</td>
</tr>
<tr>
<td>( s = \frac{\omega_s - \omega_r}{\omega_s} )</td>
<td>( f_{sl} = s f )</td>
</tr>
<tr>
<td>( %P_r = \frac{f_{sl}}{f - f_{sl}} )</td>
<td>( V_s \approx k_3 \phi_{ag} f )</td>
</tr>
<tr>
<td>( I_r \approx k_5 \phi_{ag} f_{sl} )</td>
<td>( T_{em} \approx k_6 \phi_{ag}^2 f_{sl} )</td>
</tr>
<tr>
<td>( I_m = k_8 \phi_{ag} ) (from Eq. 14-5)</td>
<td>( I_s = \sqrt{I_m^2 + I_r^2} )</td>
</tr>
</tbody>
</table>

- Not necessary for our purposes to know the exact expressions for constants used here
Torque-Speed Characteristics

Figure 14-3 A typical torque-speed characteristic; \( V_s \) and \( f \) are constant at their rated values.

- The linear part of the characteristic is utilized in adjustable speed drives.
Plot of Normalized Rotor Current

- It increases with slip and slip frequency
Acceleration Torque at Startup

\[ T_{\text{acc.}} = T_{\text{em}} - T_{\text{load}} \]

- Intersection represents the equilibrium point

**Figure 14-5** Motor start-up; \( V_s \) and \( f \) are constant at their rated values.
Torque Speed Characteristics at various Frequencies of Applied Voltage

**Figure 14-6** Torque-speed characteristics at small slip with a constant $\phi_{ag}$; constant load torque.

- The air gap flux is kept constant
Adjusting Speed of a Centrifugal Load

- The load torque is proportional to speed squared
Frequency at Startup

\[
\frac{T_{em}}{T_{rated}} \%, \quad \frac{I_r}{I_{rated}} \%
\]

\[\phi_{ag} = \text{constant, rated}\]

\[T_{start}, (I_r)_{start}\]

\[\omega_r\]

\[f_{start}\]

\[f_{sl}\]

\[\phi_{ag}\]start = f_{start}

**Figure 14-8**  Frequency at start-up.

- The torque is limited to limit current draw
Increasing Speed at Startup

- The ramp rate of frequency depends on load inertia

Figure 14-9  Ramping of frequency $f$ at start-up.
Phasor Diagram at Small Value of Slip Frequency

\begin{align*}
I_m &= -jI_m \\
\text{Figure 14-10} & \quad \text{Phasor diagram at a small value of } f_{sl}. \\
& \quad \text{• The rotor branch is assumed to be purely resistive}
\end{align*}
Voltage Boost to Keep Air Gap Flux at its Rated Value

\[ \frac{V_s}{f} = \text{constant} = \frac{(V_{s\text{ rated}})}{f_{\text{rated}}} \]

- Depends on the torque loading of the machine

**Figure 14-11** Voltage boost required to keep \( \phi_{ag} \) constant.

- Depends on the torque loading of the machine
Induction Motor Drive Capability Curves

- Mainly two regions
Generator Mode of Operation

- Rotor speeds exceed the synchronous speed

Figure 14-13  Generation mode.
Regenerative Braking Mode to Slow Down

- Machine is made to go into the generator mode

Figure 14-14  Braking (initial motor speed is $\omega_{r0}$ and the applied frequency is instantaneously decreased from $f_0$ to $f_1$).
Per-Phase Equivalent Circuit at Harmonic Frequencies

- The magnetizing branch is ignored

**Figure 14-15** Per-phase harmonic equivalent circuit.
Torque Pulsations due to Harmonics

- Rotations of fields due to the fifth and the seventh harmonics are in opposite directions.
Classification of Converter Systems

- PWM-VSI is now most commonly use
PWM-VSI System

- Diode rectifier for unidirectional power flow

Figure 14-19  PWM-VSI: (a) schematic; (b) waveforms.
PWM-VSI System

(a)

(b)

Figure 14-20  Electromagnetic braking in PWM-VSI: (a) dissipative braking; (b) regenerative braking.

• Options for recovered energy during regenerative braking
General-Purpose Speed Controller

- High dynamic performance is not the objective here

Figure 14-21 Speed control circuit. Motor speed is not measured.
Change in Switching Frequency based on the required Fundamental Frequency

- Can be significant in large power ratings

Figure 14-22  Switching frequency versus the fundamental frequency.
Field-Oriented Control

Figure 14-23  Field-oriented control for induction motor servo drive.

- A concise coverage is presented in “Advanced Electric Drives: Analysis, Control and Modeling using Simulink” by N. Mohan (www.MNPERE.com)
Square-Wave VSI Waveforms

Figure 14-24  Square-wave VSI waveforms.

- Large peak-peak ripple in currents
CSI Drives

- Mostly PWM-VSI drives are used

Figure 14-25  CSI drive: (a) inverter; (b) idealized phase waveforms.
Comparison of Three Types of Inverter Systems

Table 14-2 Comparison of Adjustable Frequency Drives

<table>
<thead>
<tr>
<th>Parameter</th>
<th>PWM</th>
<th>Square Wave</th>
<th>CSI</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input power factor</td>
<td>+</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Torque pulsations</td>
<td>++</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Multimotor capability</td>
<td>+</td>
<td>+</td>
<td>-</td>
</tr>
<tr>
<td>Regeneration</td>
<td>-</td>
<td>-</td>
<td>++</td>
</tr>
<tr>
<td>Short-circuit protection</td>
<td>-</td>
<td>-</td>
<td>++</td>
</tr>
<tr>
<td>Open-circuit protection</td>
<td>+</td>
<td>+</td>
<td>-</td>
</tr>
<tr>
<td>Ability to handle undersized motor</td>
<td>+</td>
<td>+</td>
<td>-</td>
</tr>
<tr>
<td>Ability to handle oversized motor</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Efficiency at low speeds</td>
<td>-</td>
<td>+</td>
<td>+</td>
</tr>
<tr>
<td>Size and weight</td>
<td>+</td>
<td>+</td>
<td>-</td>
</tr>
<tr>
<td>Ride-through capability</td>
<td>+</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

- PWM-VSI is by far the most commonly selected system now
Speed Control by Adjusting the Stator Voltage

- Highly inefficient in most cases

Figure 14-26  Speed control by stator voltage control:  
(a) motor with a low value of \( s_{\text{rated}} \), fan-type load;  
(b) motor with a large \( s_{\text{rated}} \), constant-torque load.
Controlling the Stator Voltage Magnitude

- Results in distorted current and torque pulsations

Figure 14-27 Stator voltage control: (a) circuit; (b) waveforms.
Torque-Speed Curves for Wound-Rotor Machines

- Highly energy-inefficient unless using energy recovery schemes

Figure 14-28 Torque–speed curves for a wound-rotor induction motor.
Figure 14-29  Static slip recovery.

- Applications in very large power ratings where the speed is to be adjusted over a very limited range.
Chapter 15
Synchronous Motor Drives

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15-2  Basic Principles of Synchronous Motor Operation  435
15-3  Synchronous Servomotor Drives with Sinusoidal Waveforms  439
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• A large variety of applications – higher efficiency
Rotor Structure

- Permanent-magnet or wound with a field winding

Figure 15-1 Structure of synchronous motors: (a) permanent-magnet rotor (two-pole); (b) salient-pole wound rotor (two-pole).
Per-Phase Representation

Figure 15-2 Per-phase representation: (a) phasor diagram; (b) equivalent circuit; (c) terminal voltage.

- In sinusoidal steady state
Phasor Diagram

- Optimum operation

Figure 15-3  Phasor diagram with

\[ \delta = 90^\circ \]
Rotor Position

- Needs closed-loop operation knowing the rotor position

Figure 15-4 Measured rotor position $\theta$ at time $t$. 
Synchronous Motor Drive

Figure 15-5 Synchronous motor servo drive.

- Controller based on steady state operation
Trapezoidal Waveform Synchronous Motor

- used in applications where speed of response not critical
Load-Commutated Inverter (LCI) Drive

- Used in very large power ratings

Figure 15-7  An LCI drive: (a) circuit; (b) idealized waveforms.
Figure 15-8  An LCI drive controller.

- Line converter controls the dc-link current
Three-Phase Cycloconverter

- Low-frequency ac output is synthesized
Chapter 16
Residential and Industrial Applications

- Significant in energy conservation; productivity
Improving Energy Efficiency of Heat Pumps

Figure 16-1  Load-proportional capacity-modulated heat pump.

- Used in one out of three new homes in the U.S.
Loss Associated with ON/OFF Cycling

- The system efficiency is improved by ~30 percent

Figure 16-2 Conventional heat pump waveforms.
Inductive Ballast of Fluorescent Lamps

- Inductor is needed to limit current

Figure 16-3  Fluorescent lamp with an inductive ballast.
Rapid-Start Fluorescent Lamps

- Starting capacitor is needed

Figure 16-4 Conventional 60-Hz rapid-start fluorescent lamp: (a) circuit schematic; (b) simplified schematic.
Electronic Ballast for Fluorescent Lamps

- Lamps operated at ~40 kHz
Induction Cooking

Figure 16-6 Induction cooking

- Pan is heated directly by circulating currents – increases efficiency
Industrial Induction Heating

- Needs sinusoidal current at the desired frequency: two options

**Figure 16-7** Induction heating: (a) voltage-source series-resonant induction heating; (b) current-source parallel-resonant induction heating.
Welding Application

- Three options

**Figure 16-8** Welders with a 60-Hz transformer: (a) controlled thyristor bridge; (b) series regulator; (c) step-down dc–dc converter.
Switch-Mode Welders

- Can be made much lighter weight

Figure 16-9 Switch-mode welder.
Integral Half-Cycle Controllers

- Used for heating

Figure 16-10 Integral half-cycle controllers: (a) three-phase circuit; (b) per-phase circuit; (c) waveforms.
Chapter 17
Electric Utility Applications

• These applications are growing rapidly
HVDC Transmission

• There are many such systems all over the world

Figure 17-1  A typical HVDC transmission system.
HVDC Poles

- Each pole consists of 12-pulse converters
HVDC Transmission: 12-Pulse Waveforms

- Idealized waveforms
HVDC Transmission: Converters

- Inverter mode of operation

Figure 17-4  Inverter mode of operating (assuming $L_e = 0$).
Control of HVDC Transmission System

- Inverter is operated at the minimum extinction angle and the rectifier in the current-control mode

Figure 17-5  Control of HVDC system.
HVDC Transmission: DC-Side Filters

Tuned for the lowest (12\textsuperscript{th} harmonic) frequency

\textbf{Figure 17-6} Filter for dc-side voltage harmonics: (a) dc-side equivalent circuit; (b) high-pass filter impedance vs. frequency.
HVDC Transmission: AC-Side Filters

Tuned for the lowest (11th and the 13th harmonic) frequencies

Figure 17-7 The ac side filters and power factor correction capacitors: (a) per-phase equivalent circuit; (b) combined per-phase filter impedance vs. frequency.
Effect of Reactive Power on Voltage Magnitude

Figure 17-8  Effect of $I_p$ and $I_q$ on $V_t$: (a) equivalent circuit; (b) change in $I_q$; (c) change in $I_p$.

- Illustration of the basic principle
Thyristor-Controlled Inductor (TCI)

Figure 17-9  A TCI, basic principle: (a) per-phase TCI; (b) 0 < α < 90°; (c) α = 120°; (d) α = 135°.

- Increasing the delay angle reduces the reactive power drawn by the TCI
Thyristor-Switched Capacitors (TSCs)

- Transient current at switching must be minimized

Figure 17-10 A TSC arrangement.
Instantaneous VAR Controller (SATCOM)

- Can be considered as a reactive current source

Figure 17-11 Instantaneous var controller.
Characteristics of Solar Cells

- The maximum power point is at the knee of the characteristics

Figure 17-12  The I–V characteristics of solar cells.
(Source: reference 10.)
Photovoltaic Interface

Figure 17-13  High-frequency photovoltaic interface.

- This scheme uses a thyristor inverter
Harnessing of Wing Energy

Figure 17-14  Interconnection of wind/hydro generator.

- A switch-mode inverter may be needed on the wind generator side also
Interface with 3-Phase Utility Grid

- Uses a thyristor inverter

Figure 17-15  New topology, utility interface [12].
Interface of SMES

- Can be used for utility load leveling

**Figure 17-16** Superconductive energy storage inductor interconnection.
Active Filters for Harmonic Elimination

- Active filters inject a nullifying current so that the current drawn from the utility is nearly sinusoidal.

**Figure 17-17** One-line diagram of an active filter.
• Power quality has become an important issue
Various Loads Supplied by the Utility Source

- PCC is the point of common coupling

Figure 18-1  Utility interface.
Diode-Rectifier Bridge

Figure 18-2  Diode rectifier bridge.

- Block diagram
Typical Harmonics in the Input Current

Table 18-1 Typical Harmonics in a Single-Phase Input Current Waveform with No Line Filtering

<table>
<thead>
<tr>
<th>$h$</th>
<th>3</th>
<th>5</th>
<th>7</th>
<th>9</th>
<th>11</th>
<th>13</th>
<th>15</th>
<th>17</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\left( \frac{I_h}{I_1} \right) %$</td>
<td>73.2</td>
<td>36.6</td>
<td>8.1</td>
<td>5.7</td>
<td>4.1</td>
<td>2.9</td>
<td>0.8</td>
<td>0.4</td>
</tr>
</tbody>
</table>

- Single-phase diode-rectifier bridge
Harmonic Guidelines: IEEE 519

Table 18-2 Harmonic Current Distortion ($I_h/I_1$)

<table>
<thead>
<tr>
<th>$I_{sc}/I_1$</th>
<th>$h &lt; 11$</th>
<th>$11 \leq h &lt; 17$</th>
<th>$17 \leq h &lt; 23$</th>
<th>$23 \leq h &lt; 35$</th>
<th>$35 \leq h$</th>
<th>Total Harmonic Distortion (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;20</td>
<td>4.0</td>
<td>2.0</td>
<td>1.5</td>
<td>0.6</td>
<td>0.3</td>
<td>5.0</td>
</tr>
<tr>
<td>20–50</td>
<td>7.0</td>
<td>3.5</td>
<td>2.5</td>
<td>1.0</td>
<td>0.5</td>
<td>8.0</td>
</tr>
<tr>
<td>50–100</td>
<td>10.0</td>
<td>4.5</td>
<td>4.0</td>
<td>1.5</td>
<td>0.7</td>
<td>12.0</td>
</tr>
<tr>
<td>100–1000</td>
<td>12.0</td>
<td>5.5</td>
<td>5.0</td>
<td>2.0</td>
<td>1.0</td>
<td>15.0</td>
</tr>
<tr>
<td>&gt;1000</td>
<td>15.0</td>
<td>7.0</td>
<td>6.0</td>
<td>2.5</td>
<td>1.4</td>
<td>20.0</td>
</tr>
</tbody>
</table>

Note: Harmonic current limits for nonlinear load connected to a public utility at the point of common coupling (PCC) with other loads at voltages of 2.4–69 kV. $I_{sc}$ is the maximum short-circuit current at PCC. $I_1$ is the maximum fundamental-frequency load current at PCC. Even harmonics are limited to 25% of the odd harmonic limits above.

Source: Reference 1.

- commonly used for specifying limits on the input current distortion
Harmonic Guidelines: IEEE 519

Table 18-3 Harmonic Voltage Limits ($V_h/V_1$) (%) for Power Producers (Public Utilities or Cogenerators)

<table>
<thead>
<tr>
<th></th>
<th>2.3–69 kV</th>
<th>69–138 kV</th>
<th>&gt; 138 kV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum for</td>
<td>3.0</td>
<td>1.5</td>
<td>1.0</td>
</tr>
<tr>
<td>individual harmonic</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total harmonic</td>
<td>5.0</td>
<td>2.5</td>
<td>1.5</td>
</tr>
<tr>
<td>distortion</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: This table lists the quality of the voltage that the power producer is required to furnish a user. It is based on the voltage level at which the user is supplied.

Source: Reference 1.

- Limits on distortion in the input voltage supplied by the utility
Reducing the Input Current Distortion

- use of passive filters

Figure 18-3  Passive filters to improve $i_s$ waveform: (a) passive filter arrangement; (b) current waveform.
Power-Factor-Correction (PFC) Circuit

- For meeting the harmonic guidelines

Figure 18-4  Active harmonic filtering: (a) step-up converter for current shaping; (b) line waveforms; (c) $v_s$ and $i_L$. 

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Power-Factor-Correction (PFC) Circuit Control

![Control block diagram]

**Figure 18-5** Control block diagram.

- generating the switch on/off signals
Power-Factor-Correction (PFC) Circuit

Figure 18-6 Constant-frequency control.

- Operation during each half-cycle
Thyristor Converters for 4-Quadrant Operation

- Two back-to-back connected 2-quadrant converters

**Figure 18-7** Back-to-back connected converters for bidirectional power flow.
Switch-Mode Converter Interface

- Bi-directional power flow; unity PF is possible

Figure 18-8 Switch-mode converter for the utility interface.
Switch-Mode Converter Interface

- Rectifier and Inverter modes based on the direction of power flow

Figure 18-9  Rectification and inversion: (a) general phasor diagram; (b) rectification at unity power factor; (c) inversion at unity power factor.
Switch-Mode Converter Control

Figure 18-10  Control of the switch-mode interface.

- DC bus voltage is maintained at the reference value
Switch-Mode Converter Interface

Figure 18-11 Waveforms in the circuit of Fig. 18-8 at unity power factor of operation: (a) phasor diagram; (b) circuit waveforms.

- Waveforms in the rectifier mode
3-Phase Switch-Mode Converter Interface

- Rectifier and Inverter modes based on the direction of power flow

Figure 18-12  Three-phase, switch-mode converter.
EMI: Conducted Interference

- Common and differential modes

**Figure 18-13** Conducted interference.
Switching Waveforms

Figure 18-14  Switching waveform.

- Typical rise and fall times
Conducted EMI

• Various Standards
Conducted EMI

Figure 18-16 Filter for conducted EMI.

- Filter arrangement
Review of Basic Semiconductor Physics
Current Flow and Conductivity

- Charge in volume $A\Delta x = \Delta Q$
  $$= q n A \Delta x = q n A v \Delta t$$

- Current density $J = (\Delta Q/\Delta t)A^{-1}$
  $$= q n v$$

- Metals - gold, platinum, silver, copper, etc.
  - $n = 10^{23} \text{ cm}^{-3}$ ; $\sigma = 10^7 \text{ mhos-cm}$

- Insulators - silicon dioxide, silicon nitride, aluminum oxide
  - $n < 10^3 \text{ cm}^{-3}$ ; $\sigma < 10^{-10} \text{ mhos-cm}$

- Semiconductors - silicon, gallium arsenide, diamond, etc.
  - $10^8 < n < 10^{19} \text{ cm}^{-3}$ ; $10^{-10} < \sigma < 10^4 \text{ mhos-cm}$
Thermal Ionization

• Si atoms have thermal vibrations about equilibrium point.

• Small percentage of Si atoms have large enough vibrational energy to break covalent bond and liberate an electron.
Electrons and Holes

- \( T_3 > T_2 > T_1 \)

- Density of free electrons
  
  \( n : \) Density of free holes \( p \)

- \( p = n = n_i(T) = \) intrinsic carrier density.

- \( n_i^2(T) = C \exp(-qE_g/(kT)) \)
  
  \( = 10^{20} \text{ cm}^{-6} \text{ at } 300 \text{ } ^\circ \text{K} \)

- \( T = \) temp in \( {^\circ} \text{K} \)

- \( k = 1.4 \times 10^{-23} \text{ joules/ } ^{\circ} \text{K} \)

- \( E_g = \) energy gap \( = 1.1 \text{ eV} \)
  
  in silicon

- \( q = 1.6 \times 10^{-19} \text{ coulombs} \)
Doped Semiconductors

- Extrinsic (doped) semiconductors: \( p = p_0 \neq n = n_0 \neq n_i \)
- Carrier density estimates:
  - Law of mass action \( n_0 p_0 = n_i^2(T) \)
  - Charge neutrality \( N_a + n_0 = N_d + p_0 \)

- P-type silicon with \( N_a \gg n_i \):
  \( p_0 \approx N_a, \ n_0 \approx n_i^2/N_a \)

- N-type silicon with \( N_d \gg n_i \):
  \( n_0 \approx N_d, \ p_0 \approx n_i^2/N_d \)
Nonequilibrium and Recombination

- **Thermal Equilibrium** - Carrier generation = Carrier recombination
  - \( n = n_o \) and \( p = p_o \)

- **Nonequilibrium** - \( n > n_o \) and \( p > p_o \)
  - \( n = n_o + \Delta n \) and \( p = n_o + \Delta n \); \( \Delta n \) = excess carrier density
  - Excess holes and excess electrons created in equal numbers by breaking of covalent bonds
  - Generation mechanisms - light (photoelectric effect), injection, impact ionization

- **Recombination** - removal of excess holes and electrons
  - Mechanisms - free electron captured by empty covalent bond (hole) or trapped by impurity or crystal imperfection
  - Rate equation: \( \frac{d(\Delta n)}{dt} = -\frac{\Delta n}{\tau} \)
  - Solution \( \Delta n = \Delta n(0)e^{-t/\tau} \)
Carrier Lifetimes

- \( \tau \) = excess carrier lifetime
  - Usually assumed to be constant. Changes in two important situations.
  - \( \tau \) increases with temperature \( T \)
  - \( \tau \) decreases at large excess carrier densities; \( \tau = \tau_0/[1 + (n/n_b)^2] \)

- Control of carrier lifetime values.
  - Switching time-on state loss tradeoff mandates good lifetime control.
  - Control via use of impurities such as gold - lifetime killers.
  - Control via electron irradiation - more uniform and better control.
**Current Flow**

**Drift**
- $J_{\text{drift}} = q \mu_n n E + q \mu_p p E$
- $\mu_n = 1500 \text{ cm}^2/\text{V-sec}$ for silicon at room temp. and $N_d < 10^{15} \text{ cm}^{-3}$
- $\mu_p = 500 \text{ cm}^2/\text{V-sec}$ for silicon at room temp. and $N_a < 10^{15} \text{ cm}^{-3}$

**Diffusion**
- $J_{\text{diff}} = J_n + J_p = q D_n dn/dx - q D_p dp/dx$
- $D_n/\mu_n = D_p/\mu_p = kT/q$; Einstein relation
- $D =$ diffusion constant, $\mu =$ carrier mobility

**Total current density** $J = J_{\text{drift}} + J_{\text{diff}}$
PN Junction

metallurgical junction

Step (abrupt) junction

Linearly graded junction
Formation of Space Charge Layer

- Diffusing electrons and holes leave the region near metallurgical junction depleted of free carriers (depletion region).
- Exposed ionized impurities form space charge layer.
- Electric field due to space charge opposes diffusion.
Quantitative Description of Space Charge Region

- Assume step junction.

\[
\frac{d^2 \Phi}{dx^2} = - \Phi
\]

\[
\Phi = -qN_a \quad ; \quad x < 0
\]

\[
\Phi = qN_d \quad ; \quad x > 0
\]

\[
\frac{d \Phi}{dx} = -E(x)
\]

\[
E(x) = \frac{qN_a(x+x_p)}{\Phi}; \quad -x_p < x < 0
\]

\[
E(x) = \frac{qN_d(x-x_n)}{\Phi}; \quad 0 < x < x_n
\]

\[
\Phi_c = \int_{-x_p}^{x_n} E(x) \, dx
\]

\[
\Phi_c = -qN_a x_p^2 + qN_d x_n^2
\]
Contact (Built-in, Junction) Potential

- In thermal equilibrium $J_n = q \mu_n n \frac{dn}{dx} + q D_n \frac{dn}{dx} = 0$

- Separate variables and integrate; $\frac{n(x_n)}{n(x_p)} = -\frac{D_n}{\mu_n} \frac{dn}{n}$

- $n(x_n) - n(x_p) = c = \frac{kT}{q} \ln \frac{N_a N_d}{n_i^2}$; $c$ = contact potential

- Example
  - Room temperature $kT/q = 0.025$ eV
  - $N_a = N_d = 10^{16}$ cm$^{-3}$ ; $n_i^2 = 10^{20}$ cm$^{-6}$
  - $F_c = 0.72$ eV
Reverse-Biased Step Junction

- Starting equations
  - \( W(V) = x_n(V) + x_p(V) \)
  - \( V + \frac{q}{2} = -\frac{qN_a x_p^2 + qN_d x_n^2}{2} \)
  - Charge neutrality \( qN_a x_p = qN_d x_n \)

- Solve equations simultaneously
  - \( W(V) = W_0 \sqrt{1 + \frac{V}{\frac{q}{2}}} \)
  - \( W_0 = \sqrt{\frac{2q}{2} \left( \frac{N_a + N_d}{qN_a N_d} \right)} \)
  - \( E_{\text{max}} = \frac{2q}{W_0} \sqrt{1 + \frac{V}{\frac{q}{2}}} \)
Forward-Biased PN Junction

• Forward bias favors diffusion over drift.

• Excess minority carrier injection into both p and n drift regions.

• Minority carrier diffusion lengths.
  • \( L_n = [D_n D_n]^{0.5} \)
  • \( L_p = [D_p D_p]^{0.5} \)
Ideal PN Junction I-V Characteristics

- Excess carriers in drift regions recombined and thus more must be constantly injected if the distributions $n_p(x)$ and $p_n(x)$ are to be maintained.

- Constant injection of electrons and holes results in a current density $J$ given by

$$ J = \frac{Q_n}{\hbar} + \frac{Q_p}{\hbar} = q n_i^2 \left[ \frac{L_n}{N_a \hbar} + \frac{L_p}{N_d \hbar} \right] \exp\left(\frac{qV}{kT}\right) - 1 $$

$$ J = J_s \left[ \exp\left(\frac{qV}{kT}\right) - 1 \right] ; \quad J_s = q n_i^2 \left[ \frac{L_n}{N_a \hbar} + \frac{L_p}{N_d \hbar} \right] $$

\[ \text{forward bias} \quad \text{reverse bias} \quad \text{combined characteristic} \]
Reverse Saturation Current

- Carrier density gradient immediately adjacent to depletion region causes reverse saturation current to flow via diffusion.

- $J_s$ independent of reverse voltage $V$ because carrier density gradient unaffected by applied voltage.

- $J_s$ extremely temperature sensitivity because of dependence on $n_i^2(T)$.
Impact Ionization

- \( E \geq E_{BD} \); free electron can acquire sufficient from the field between lattice collisions (\( t_c \approx 10^{-12} \text{ sec} \)) to break covalent bond.

- Energy: \( 0.5mv^2 = qE_g; v = qE_BDt_c \)

- Solving for \( E_{BD} \) gives
  \[
  E_{BD} = \sqrt{\frac{2E_g m}{q t_c^2}}
  \]
  
  - Numerical evaluation
    - \( m = 10^{-27} \text{ grams}, E_g = 1.1 \text{ eV}, t_c = 10^{-12} \text{ sec.} \)

    - \( E_{BD} = \sqrt{\frac{(2)(1.1)(10^{27})}{(1.6\times10^{-19})(10^{-24})}} = 3\times10^5 \text{ V/cm} \)

    - Experimental estimates are 2-3.5\( \times10^5 \) V/cm
Lecture Notes

Diodes for Power Electronic Applications

OUTLINE

• PN junction power diode construction
• Breakdown voltage considerations
• On-state losses
• Switching characteristics
• Schottky diodes
• Modeling diode behavior with PSPICE
Basic Structure of Power Semiconductor Diodes

Anode

P+  \( N_A = 10^{19} \text{ cm}^{-3} \)

N- epi  \( N_D = 10^{14} \text{ cm}^{-3} \)

N+ substrate  \( N_D = 10^{19} \text{ cm}^{-3} \)

breakdown voltage dependent

10 microns

250 microns

anode

cathode

\( V_{BD} \)

\( 1 \text{ V} \)

\( \frac{1}{R_{on}} \)

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Breakdown Voltage Estimate - Step Junction

- Non-punch-through diode. Drift region length \( W_d > W(BV_{BD}) = \) length of space charge region at breakdown.

- \( W(V) = W_0 \sqrt{1 + V / \Phi_c} \)

- \( W_0 = \sqrt{ \frac{2 \Phi_c (N_a + N_d)}{q N_a N_d} } \)

- \( E_{\text{max}} = \frac{2 \Phi_c}{W_0} \sqrt{1 + \frac{V}{\Phi_c}} \)

- Power diode at reverse breakdown: \( N_a >> N_d ; E = E_{\text{BD}} ; V = BV_{BD} \gg \Phi_c \)

- \( W^2(BV_{BD}) = \frac{W_0^2 \ BV_{BD}}{\Phi_c} ; W_0^2 = \frac{2 \Phi_c}{q \ N_d} \)

- Conclusions
  1. Large \( BV_{BD} (10^3 \ V) \) requires \( N_d < 10^{15} \ cm^{-3} \)
  2. Large \( BV_{BD} (10^3 \ V) \) requires \( N^- \) drift region > 100 \( \mu m \)
Breakdown Voltage - Punch-Through Step Junction

- Punch-through step junction - $W(BV_{BD}) > W_d$

\[ E_1 = \frac{qN_d W_d}{\Box} ; \quad V_1 = \frac{qN_d W_d^2}{2\Box} \]

- $V_2 = E_2 W_d$

- At breakdown:
  - $V_1 + V_2 = BV_{BD}$
  - $E_1 + E_2 = E_{BD}$

- $BV_{BD} = E_{BD} W_d - \frac{qN_d W_d^2}{2\Box}$

- If $N_d << \frac{\Box(E_{BD})^2}{2q(BV_{BD})}$ (required value of $N_d$ for non-punch-thru diode), then
  - $BV_{BD} \approx E_{BD} W_d$ and
  - $W_d(Punch-thru) \approx 0.5 W_d(non-punch-thru)$
Effect of Space Charge Layer Curvature

- Impurities diffuse as fast laterally as vertically.

- Curvature develops in junction boundary and in depletion layer.

- If radius of curvature is comparable to depletion layer thickness, electric field becomes spatially nonuniform.

- Spatially nonuniform electric field reduces breakdown voltage.

- $R > 6 \, W(BV_{BD})$ in order to limit breakdown voltage reduction to 10% or less.

- Not feasible to keep $R$ large if $BV_{BD}$ is to be large ($> 1000 \, V$).
Control of Space Charge Layer Boundary Contour

- Electrically isolated conductors (field plates) act as equipotential surfaces.
- Correct placement can force depletion layer boundary to have larger radius of curvature and thus minimize field crowding.
- Electrically isolated p-regions (guard rings) have depletion regions which interact with depletion region of main pn junction.
- Correct placement of guard rings can result in composite depletion region boundary having large radius of curvature and thus minimize field crowding.
Surface Contouring to Minimize Field Crowding

- Large area diodes have depletion layers that contact Si surface.
- Difference in dielectric constant of Si and air causes field crowding at surface.
- Electric fields fringing out into air attract impurities to surface that can lower breakdown voltage.

- Proper contouring of surface can minimize depletion layer curvature and thus field crowding.
- Use of a passivation layer like SiO₂ can also help minimize field crowding and also contain fringing fields and thus prevent attraction of impurities to surface.
Conductivity Modulation of Drift Region

- Forward bias injects holes into drift region from P+ layer. Electrons attracted into drift region from N+ layer. So-called double injection.

- If $W_d \leq$ high level diffusion length $L_a$, carrier distributions quite flat with $p(x) \approx n(x) \approx n_a$.

- For $n_a >>$ drift region doping $N_d$, the resistance of the drift region will be quite small. So-called conductivity modulation.

- On-state losses greatly reduced below those estimated on basis of drift region low-level ($N_d$) ohmic conductivity.
Drift Region On-State Voltage Estimate

- $I_F = \frac{Q_F}{q} = \frac{q A W_d n_a}{W_d}$; Current needed to maintain stored charge $Q_F$.

- $I_F = \frac{q \left[ \mu_n + \mu_p \right] n_a A V_d}{W_d}$; Ohm’s Law ($J = \frac{E}{L}$)

- $V_d = \frac{W_d^2}{\left[ \mu_n + \mu_p \right]}$; Equate above two equations and solve for $V_d$

- Conclusion: long lifetime $\min$imizes $V_d$. 
Diode On-State Voltage at Large Forward Currents

- \( \mu_n + \mu_p = \frac{\mu_o}{1 + \frac{n_a}{n_b}} \); \( n_b \approx 10^{17} \text{ cm}^{-3} \).

- Mobility reduction due to increased carrier-carrier scattering at large \( n_a \).

- \( I_F = \frac{q n_a A V_d}{W_d} \frac{\mu_o}{1 + \frac{n_a}{n_b}} \); Ohms Law with density-dependent mobility.

- Invert Ohm’s Law equation to find \( V_d \) as function \( I_F \) assuming \( n_a >> n_b \).

\begin{align*}
\text{Vd} &= \frac{I_F W_d}{q \mu_o n_b A} \\
\text{Vd} &= I_F \text{Ron} \\
\text{V} &= \text{Vj} + \text{Vd}
\end{align*}
Diode Switching Waveforms in Power Circuits

- \( \frac{\text{di}_F}{\text{dt}} \) and \( \frac{\text{di}_R}{\text{dt}} \) determined by external circuit.
- Inductances or power semiconductor devices.

\[
S = \frac{t_5}{t_4}
\]
Diode Internal Behavior During Turn-on

\[ C_{sc}(V) = \frac{\Delta A}{W(V)} \]

\[ R_d = \frac{W_d}{q \frac{\Delta n}{n \cdot N_d} \cdot A} \]

\[ V_{FP} \approx I_F \frac{R_d}{R_d} + L \frac{di_F}{dt} \]

\[ L = \text{stray or wiring inductance} \]

- Injection of excess carriers into drift region greatly reduces \( R_d \).

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Diode Internal Behavior During Turn-off

- $R_d$ increases as excess carriers are removed via recombination and carrier sweep-out (negative current).

- $V_r = I_{rr}R_d + L\frac{di_R}{dt}$

- Insufficient excess carriers remain to support $I_{rr}$, so $P^+N^-$ junction becomes reverse-biased and current decreases to zero.

- Voltage drops from $V_{rr}$ to $V_R$ as current decreases to zero. Negative current integrated over its time duration removes a total charge $Q_{rr}$. 

$t_s$ interval
Factors Effecting Reverse Recovery Time

- \( I_{rr} = \frac{dI_r}{dt} t_4 = \frac{dI_r}{dt} \frac{t_{rr}}{(S + 1)} \); Defined on switching waveform diagram

- \( Q_{rr} = \frac{I_{rr} \cdot t_{rr}}{2} = \frac{dI_r}{dt} \frac{t_{rr}^2}{2(S + 1)} \); Defined on waveform diagram

- Inverting \( Q_{rr} \) equation to solve for \( t_{rr} \) yields

\[
t_{rr} = \sqrt{\frac{2Q_{rr}(S+1)}{dI_r/dt}}\]

and

\[
I_{rr} = \sqrt{\frac{2Q_{rr}dI_r}{dt}} \quad \frac{dI_r}{dt} \quad (S + 1)
\]

- If stored charge removed mostly by sweep-out \( Q_{rr} \approx Q_F \approx I_F \)

- Using this in eqs. for \( I_{rr} \) and \( t_{rr} \) and assuming \( S + 1 \approx 1 \) gives

\[
t_{rr} = \sqrt{\frac{2 I_F}{dI_r/dt}} \quad \text{and}
\]

\[
I_{rr} = \sqrt{\frac{2 I_F}{dI_r/dt}}
\]
Carrier Lifetime-Breakdown Voltage Tradeoffs

- Low on-state losses require
  \[
  L = \sqrt{D} = \sqrt{\frac{kT}{q [\mu_n + \mu_p]}}
  \]
  \[
  L = W_d \geq W(V) = 10^{-5}BV_{BD}
  \]

- Solving for the lifetime yields
  \[
  \frac{W_d^2}{(kT/q) [\mu_n+\mu_p]} = 4 \times 10^{-12} (BV_{BD})^2
  \]

- Substituting for \( \frac{W_d^2}{W(V)} \) in \( I_{rr} \) and \( t_{rr} \) equations gives
  - \( t_{rr} = 2.8 \times 10^{-6} BV_{BD} \sqrt{\frac{I_F}{(di_R/dt)}} \)
  - \( I_{rr} = 2.8 \times 10^{-6} BV_{BD} \sqrt{I_F \frac{di_R}{dt}} \)

Conclusions

1. Higher breakdown voltages require larger lifetimes if low on-state losses are to be maintained.
2. High breakdown voltage devices slower than low breakdown voltage devices.
3. Turn-off times shortened by large \( \frac{di_R}{dt} \) but \( I_{rr} \) is increased.
Schottky Diodes

Characteristics

• $V(\text{on}) = 0.3 - 0.5$ volts.

• Breakdown voltages $\leq 100-200$ volts.

• Majority carrier device - no stored charge.

• Fast switching because of lack of stored charge.
Physics of Schottky Diode Operation

- Electrons diffuse from Si to Al because electrons have larger average energy in silicon compared to aluminum.

- Depletion layer and thus potential barrier set up. Gives rise to rectifying contact.

- No hole injection into silicon. No source of holes in aluminum. Thus diode is a majority carrier device.

- Reverse saturation current much larger than in pn junction diode. This leads to smaller $V_{on}$ (0.3 - 0.5 volts)
Schottky Diode Breakdown Voltage

- Breakdown voltage limited to 100-200 volts.

- Narrow depletion region widths because of heavier drift region doping needed for low on-state losses.

- Small radius of curvature of depletion region where metallization ends on surface of silicon. Guard rings help to mitigate this problem.

- Depletion layer forms right at silicon surface where maximum field needed for breakdown is less because of imperfections, contaminants.
Schottky Diode Switching Waveforms

- Schottky diodes switch much faster than pn junction diodes. No minority carrier storage.

- Forward voltage overshoot $V_{FP}$ much smaller in Schottky diodes. Drift region ohmic resistance $R_{\text{W}}$.

- Reverse recovery time $t_{rr}$ much smaller in Schottky diodes. No minority carrier storage.

- Reverse recovery current $I_{rr}$ comparable to pn junction diodes. Space charge capacitance in Schottky diode larger than in pn junction diode because of narrower depletion layer widths resulting from heavier dopings.

\[ C(\text{Schottky}) \approx 5 \ C(\text{PN}) \]

\[ R_{\text{W}} \ (\text{Sch.}) \ll R_{\text{W}} \ (\text{pn}) \]
Ohmic Contacts

- Electrons diffuse from Al into p-type Si because electrons in Al have higher average energy.

- Electrons in p-type Si form an accumulation layer of greatly enhanced conductivity.

- Contact potential and rectifying junction completely masked by enhanced conductivity. So-called ohmic contact.

- In N⁺ Si depletion layer is very narrow and electric fields approach impact ionization values. Small voltages move electrons across barrier easily because quantum mechanical tunneling occurs.
PN Vs Schottkys at Large BVBD

• Minority carrier drift region relationships
  • \( I_F \approx \frac{q \left[ \mu_n + \mu_p \right] n_a A V_d}{W_d} \)

• Maximum practical value of \( n_a = 10^{17} \) cm\(^{-3}\) and corresponding to
  \( \mu_n + \mu_p = 900 \) cm\(^2\)/(V-sec)

• Desired breakdown voltage requires
  \( W_d \geq 10^{-5} \) BV\(_{BD}\)
  \( \frac{I_F}{A} = 1.4 \times 10^6 \frac{V_d}{BV_{BD}} \)

• Majority carrier drift region relationships
  • \( I_F \approx \frac{q \left[ \mu_n + \mu_p \right] N_d A V_d}{W_d} \)

• Desired breakdown voltage requires \( N_d = \frac{1.3 \times 10^{17}}{BV_{BD}} \) and
  \( W_d \geq 10^{-5} \) BV\(_{BD}\)

• Large BV\(_{BD}\) (1000 V) requires \( N_d = 10^{14} \) cm\(^{-3}\) where \( \mu_n + \mu_p = 1500 \) cm\(^2\)/(V-sec)

  \( \frac{I_F}{A} \approx 3.1 \times 10^6 \frac{V_d}{[BV_{BD}]^2} \)

• Conclusion: Minority carrier devices have lower on-state losses at large BV\(_{BD}\).
PSPICE Built-in Diode Model

- **Circuit diagram**

- **Components**
  - $C_j$ - nonlinear space-charge capacitance
  - $C_d$ - diffusion capacitance. Caused by excess carriers. Based on quasi-static description of stored charge in drift region of diode.
  - Current source $i_{dc}(v_j)$ models the exponential I-V characteristic.
  - $R_s$ accounts for parasitic ohmic losses at high currents.

\[
\begin{align*}
  v_{\text{diode}} &= v_j + R_s i_{\text{diode}} \\
  v_{\text{diode}} &= v_j + R_s i_{\text{diode}}
\end{align*}
\]
Stored Charge in Diode Drift Region - Actual Versus Quasi-static Approximation

- One dimensional diagram of a power diode.

- Quasistatic view of decay of excess carrier distribution during diode turn-off. $n(x,t) = n(x=0,t) f(x)$

- Redistribution of excess carriers via diffusion ignored. Equivalent to carriers moving with infinite velocity.

- Actual behavior of stored charge distribution during turn-off.
Example of Faulty Simulation Using Built-in Pspice Diode Model

- Test circuit example - step-down converter.
- PSPICE diode model parameters - (TT=100ns Cjo=100pF Rs=.004 Is=20fA)

- Diode voltage transient
- Diode current transient.
Improved (lumped-charge) Diode Model

• More accurately model distributed nature of excess carrier distribution by dividing it into several regions, each described by a quasi-static function. Termed the lumped-charge approach.

• Circuit diagram of improved diode model. Circuit written in terms of physical equations of the lumped-charge model.

• Detailed equations of model given in subcircuit listing.
• Many other even better (but more complicated models available in technical literature)..
Details of Lumped-Charge Model

Subcircuit Listing

```
.Subckt DMODIFY 1 9 Params: Is1=1e-6, Ise=1e-40, Tau=100ns, +Tm=100ns,Rmo=Rs=.001, Vta=.0259, CAP=100p, Gde=.5, + Fbcoeff=.5, Phi=1, Irbk=1e20,Vrbk=1e20
*Node 1= anode and Node 9 = cathode
Dcj 1 2 Dcap : Included for space charge capacitance and reverse
*breakdown.
.model Dcap D (Is=1e-25 Rs=0 TT=0 Cjo={CAP} M={Gde}
+FC={Fbcoeff} Vj={Phi} +IBV={Irbk} BV=Vrbk})
Gd 1 2 Value={((v(5)-v(6))/Tm +Ise*(exp(v(1,2)/Vta)-1)}
*Following components model forward and reverse recovery.
Ee 5 0 VALUE = {Is1*Tau*(exp(V(1,2)/(2*Vta))-1)}; Ee=Qe
Re 5 0 1e6
Em 6 0 VALUE = {(V(5)/Tm-i(Vsense1))*Tm*Tau/(Tm+Tau)}
*Em=Qm
Rm 6 0 1e6
Edm 7 0 VALUE = {v(6)};Edm=Qm
Vsense1 7 8 dc 0 ; i(vsense1)=dQm/dt
Cdm 8 0 1
Rdm 8 0 1e9
Rs 2 3 4e-3
Emo 3 4 VALUE=(2*Vta*Rmo*Tm*i(Vsense2)
+/(v(6)*Rmo+Vta*Tm)); Vm
Vsense2 4 9 dc 0
.ends
```

- Symbolize subcircuit listing into SCHEMATICS using SYMBOL WIZARD
- Pass numerical values of parameters Tau, Tm, Rmo, Rs, etc. by entering values in PART ATTRIBUTE window (called up within SCHEMATICS).
- See reference shown below for more details and parameter extraction procedures.
Simulation Results Using Lumped-Charge Diode Model

Diode voltage and current waveforms

Simulation Circuit

- Note soft reverse recovery and forward voltage overshoot. Qualitatively matches experimental measurements.
Bipolar Junction Transistors (BJTs)

Outline

- BJT structure and I-V characteristics
- Physical operation of power BJTs
- Switching characteristics
- Breakdown voltage
- Second breakdown
- On-state voltage
- Safe operating areas
Basic Geometry of Power BJTs

Features to Note

- Multiple narrow emitters - minimize emitter current crowding.
- Multiple parallel base conductors - minimize parasitic resistance in series with the base.
BJT Construction Parameters

Features to Note

- Wide base width - low (<10) beta.
- Lightly doped collector drift region - large breakdown voltage.
Darlington-connected BJTs

\[ I_C = \frac{I_C}{I_B} = I_D I_{M+} I_{D+} I_M \]

- Composite device has respectable beta.
Features to Note

- 2nd breakdown - must be avoided.
- Quasi-saturation - unique to power BJTs
- $BV_{CBO} > BV_{CEO}$ - extended blocking voltage range.
BJT Internal Current Components

- $I_{ne}$ and $I_{pe}$ flow via diffusion. $I_{nc}$ and $I_{pc}$ flow via drift.

- $I_{ne} \gg I_{pe}$ because of heavy emitter doping.

- $I_{ne} \approx I_{nc}$ because $L_{nb} = \{D_{nb} \cdot \mu_{nb}\}^{1/2} << W_{base}$ and collector area much larger than emitter area.

- $I_{pc} <<$ other current components because very few holes in b-c space charge region.
Power BJT Current Gain

- $I_C \approx I_{nc}$ since $I_{pc}$ very small: $I_B = -I_C - I_B = -I_{nc} + I_{ne} + I_{pe}$

- $I_B / I_C = 1/\alpha = (I_{ne} - I_{nc}) / I_{nc} + I_{pe} / I_{nc}$

- $(I_{ne} - I_{nc}) / I_{nc}$ represents fraction of electrons injected into base that recombine in the base. Minimize by having large values of $\overline{\delta_{hb}}$ (for long diffusion lengths) and short base widths $W_{base}$

- $I_{pe}$ proportional to $p_{no} = (n_i)^2 / N_{de}$; Minimize via large $N_{de}$

- Short base width conflicts with need for larger base width needed in HV BJTs to accommodate CB depletion region.

- Long base lifetime conflicts with need for short lifetime for faster switching speeds

- Trade-offs (compromises) in these factors limit betas in power BJTs to range of 5 to 20
Beta decrease at large collector current due to high level injection effects (conductivity modulation where $d_n = d_p$) in base.

- When $d_n = d_p$, base current must increase faster than collector current to provide extra holes. This constitutes a reduction in beta.

- High level injection conditions aided by emitter current crowding.
Emitter Current Crowding

- $I_B$ proportional to $\exp\left\{ \frac{qV_{BE}}{kT} \right\}$
- Later voltage drops make $V_{BE}$ larger at edge of emitters.
- Base/emitter current and thus carrier densities larger at edge of emitters. So-called emitter current crowding.
- This emitter current crowding leads to high level injection at relatively modest values of current.
- Reduce effect of current crowding by breaking emitters into many narrow regions connected electrically in parallel.
Quasi-saturation in Power BJTs

Power BJT

Active region

\( V_{BC} < 0 \)

Quasi-saturation

\( V_{BC} > 0 \) but drift region not completely filled with excess carriers.

Hard saturation

\( V_{BC} > 0 \) and drift region filled with excess carriers.

- Beta decreases in quasi-saturation because effective base width (virtual base) width has increased.
Generic BJT Application - Clamped Inductive Load

- Current source $I_o$ models an inductive load with an L/R time constant $\gg$ than switching period.

- Positive base current turns BJT on (hard saturation). So-called forward bias operation.

- Negative base current/base-emitter voltage turns BJT off. So-called reverse bias operation.

- Free wheeling diode DF prevents large inductive overvoltage from developing across BJT collector-emitter terminals.
Power BJT Turn-on Waveforms

- $i_B(t)$
- $v_{BE}(t)$
- $i_C(t)$
- $v_{CE}(t)$

Key parameters:
- $t_{d,on}$
- $V_{BE,on}$
- $t_{ri}$
- $V_{BE,off}$
- $I_{B,on}$
- $I_o$
- $V_{dc}$
- $t_{fv1}$
- $t_{fv2}$
- $V_{CE,sat}$

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Excess Carrier Growth During BJT Turn-on

- Growth of excess carrier distributions begins after $t_{d(on)}$ when B-E junction becomes forward biased.
- Entrance into quasi-saturation discernable from voltage or current waveform at start of time $t_{vf2}$.
- Collector current “tailing” due to reduced beta in quasi-saturation as BJT turns off.
- Hard saturation entered as excess carrier distribution has swept across drift region.
Turn-off Waveforms with Controlled Base Current

- Base current must make a controlled transition (controlled value of \(-\frac{di_B}{dt}\)) from positive to negative values in order to minimize turn-off times and switching losses.
Controlled Turn-off Excess Carrier Removal

- $t_s$ = storage time = time required to remove excess charge $Q_3$.
- $t_{rv1}$ = time to remove charge $Q_2$ holding transistor in quasi-saturation.
- $t_{rv2}$ = time required for $V_{CE}$ to complete its growth to $V_{dc}$ with BJT in active region.
- $t_{fi}$ = time required to remove remaining stored charge $Q_1$ in base and each edge of cut-off.
Turn-off Waveforms with Uncontrolled Base Current

- Excessive switching losses with collector current tailing.
Uncontrolled Turn-off Excess Carrier Removal

- Uncontrolled base current removes stored charge in base faster than in collector drift region.
- Base-emitter junction reverse biased before collector-base junction.
- Stored charge remaining in drift region now can be only removed by the negative base current rather than the much larger collector current which was flowing before the B-E junction was reverse biased.
- Takes longer time to finish removal of drift region stored charge thus leading to collector current “tailing” and excessive switching losses.
Darlington Switching Behavior

- Turn-on waveforms for Darlington very similar to single BJT circuit.
- Turn-on times somewhat shorter in Darlington circuit because of large base drive for main BJT.
- Turn-off waveforms significantly different for Darlington.
- Diode $D_1$ essential for fast turn-off of Darlington. With it, $Q_M$ would be isolated without any negative base current once $Q_D$ was off.
- Open base turn-off of a BJT relies on internal recombination to remove excess carriers and takes much longer than if carriers are removed by carrier sweepout via a large collector current.
Darlington Turn-off Waveforms

\[ i_{B,\text{on}}(t) \rightarrow -\frac{di_B}{dt} \rightarrow i_{B,\text{off}}(t) \]

\[ v_{\text{BE,off}} \rightarrow V_{\text{CE,\text{sat}}} \rightarrow V_{\text{dc}} \]

\[ Q_D \text{ off} \quad Q_D \& Q_M \text{ on} \]

\[ I_o \]

\[ \text{CE,sat} \]

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Power BJT Breakdown Voltage

- Blocking voltage capability of BJT limited by breakdown of CB junction.
  - $BV_{CBO} = CB$ junction breakdown with emitter open.
  - $BV_{CEO} = CB$ junction breakdown with base open.
  - $BV_{CEO} = BV_{CBO}/(\text{[factor]}^{1/n}; n = 4$ for npn BJTs and $n = 6$ for PNP BJTs

- BE junction forward biased even when base current $= 0$ by reverse current from CB junction.

- Excess carriers injected into base from emitter and increase saturation current of CB junction.

- Extra carriers at CB junction increase likelihood of impact ionization at lower voltages, thus decreasing breakdown voltage.

- Wide base width to lower beta and increase $BV_{CEO}$.

- Typical base widths in high voltage (1000V) BJTs $= 5$ to 10 and $BV_{CEO} = 0.5 \times BV_{CBO}$. 
Avoidance of Reach-thru

- Large electric field of depletion region will accelerate electrons from emitter across base and into collector. Resulting large current flow will create excessive power dissipation.

- Avoidance of reach-thru
  - Wide base width so depletion layer width less than base width at CB junction breakdown.
  - Heavier doping in base than in collector so that most of CB depletion layer is in drift region and not in the base.
Second Breakdown

- 2nd breakdown during BJT turn-off in step-down converter circuit.

- Precipitous drop in C-E voltage and perhaps rise in collector current.

- Simultaneous rise in highly localized regions of power dissipation and increases in temperature of same regions.
  1. Direct observations via infrared cameras.
  2. Evidence of crystalline cracking and even localized melting.

- Permanent damage to BJT or even device failure if 2nd breakdown not terminated within a few µsec.
2nd Breakdown and Current Density Nonuniformities

- Minority carrier devices prone to thermal runaway.
  - Minority carrier density proportional to $n_i(T)$ which increases exponentially with temperature.
  - If constant voltage maintained across a minority carrier device, power dissipation causes increases in temp. which in turn increases current because of carrier increases and thus better conduction characteristic.
  - Increase in current at constant voltage increases power dissipation which further increases temperature.
  - Positive feedback situation and potentially unstable. If temp. continues to increase, situation termed thermal runaway.

- Current densities nonuniformities in devices an accentuate problems.
  - Assume $J_A > J_B$ and $T_A > T_B$
  - As time proceeds, differences in $J$ and $T$ between regions A and B become greater.
  - If temp. on region A gets large enough so that $n_i >$ majority carrier doping density, thermal runaway will occur and device will be in 2nd breakdown.
Current Crowding Enhancement of 2nd Breakdown Susceptibility

- Emitter current crowding during either turn-on or turn-off accentuates propensity of BJTs to 2nd breakdown.

- Minimize by dividing emitter into many narrow areas connected electrically in parallel.
**Velocity Saturation and Second Breakdown**

- Moderate current in drift region - BJT active.
- Electric field $E_1 = J_c/(q\mu_nN_d) < E_{sat}$

- Large current density in drift region - BJT active.
- $J_c > q\mu_nN_d E_{sat}$. Extra electrons needed to carry extra current.
- Negative space density gives rise to nonuniform electric field.
- $E_{max}$ may exceed impact ionization threshold while total voltage $< BV_{CEO}$. 
Contributions to BJT On-State Losses

- $P_{on} = I_C \cdot V_{CE,\text{sat}}$

- $V_{CE,\text{sat}} = V_{BE,\text{sat}} - V_{BC,\text{sat}} + V_d + I_C(R_c + R_e)$

- $V_{BE,\text{sat}} - V_{BC,\text{sat}}$ typically 0.1-0.2 V at moderate values of collector current.

- Rise in $V_{BE,\text{sat}} - V_{BC,\text{sat}}$ at larger currents due to emitter current crowding and conductivity modulation in base.
BJT Safe Operating Areas

Forward bias safe operating area

Reverse bias safe operating area

switching trajectory of diode-clamped inductive load circuit

T$_{j,\text{max}}$

2nd breakdown

V$_{BE,\text{off}} < 0$

V$_{BE,\text{off}} = 0$

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Lecture Notes

Power MOSFETs

Outline

• Construction of power MOSFETs
• Physical operations of MOSFETs
• Power MOSFET switching Characteristics
• Factors limiting operating specifications of MOSFETs
• COOLMOS
• PSPICE and other simulation models for MOSFETs
Multi-cell Vertical Diffused Power MOSFET (VDMOS)
Important Structural Features of VDMOS

1. Parasitic BJT. Held in cutoff by body-source short

2. Integral anti-parallel diode. Formed from parasitic BJT.

3. Extension of gate metallization over drain drift region. Field plate and accumulation layer functions.

4. Division of source into many small areas connected electrically in parallel. Maximizes gate width-to-channel length ratio in order to increase gain.

5. Lightly doped drain drift region. Determines blocking voltage rating.
Alternative Power MOSFET Geometries

- Trench-gate MOSFET
  - Newest geometry. Lowest on-state resistance.

- V-groove MOSFET.
  - First practical power MOSFET.
  - Higher on-state resistance.
MOSFET I-V Characteristics and Circuit Symbols

N-channel MOSFET

P-channel MOSFET

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The Field Effect - Basis of MOSFET Operation

Threshold Voltage $V_{GS(th)}$

- $V_{GS}$ where strong inversion layer has formed. Typical values 2-5 volts in power MOSFETs

Value determined by several factors:
1. Type of material used for gate conductor
2. Doping density of body region directly beneath gate
3. Impurities/bound charges in oxide
4. Oxide capacitance per unit area $C_{ox} = \frac{\square}{t_{ox}}$
   
   $t_{ox} = \text{oxide thickness}$

- Adjust threshold voltage during device fabrication via an ion implantation of impurities into body region just beneath gate oxide.
Drift Velocity Saturation

- In MOSFET channel, \( J = q \mu_n n E \)
  \[ = q n v_n \]
  velocity \( v_n = \mu_n E \)

- Velocity saturation means that the mobility \( \mu_n \) inversely proportional to electric field \( E \).

- Mobility also decreases because large values of \( V_{GS} \) increase free electron density.

- At larger carrier densities, free carriers collide with each other (carrier-carrier scattering) more often than with lattice and mobility decreases as a result.

- Mobility decreases, especially via carrier-carrier scattering lead to linear transfer curve in power devices instead of square law transfer curve of logic level MOSFETs.

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Channel-to-Source Voltage Drop

- $V_{GS} = V_{GG} = V_{ox} + V_{CS(x)}$;
  $V_{CS(x)} = I_{D1}R_{CS(x)}$

- Larger $x$ value corresponds to being closer to the drain and to a smaller $V_{ox}$.

- Smaller $V_{ox}$ corresponds to a smaller channel thickness. Hence reduction in channel thickness as drain is approached from the source.
Channel Pinch-off at Large Drain Current

- $I_{D2} > I_{D1}$ so $V_{CS2(x)} > V_{CS1(x)}$ and thus channel narrower at an given point.

- Total channel resistance from drain to source increasing and curve of $I_D$ vs $V_{DS}$ for a fixed $V_{GS}$ flattens out.

- Apparent dilemma of channel disappearing at drain end for large $I_D$ avoided.

1. Large electric field at drain end oriented parallel to drain current flow. Arises from large current flow in channel constriction at drain.

2. This electric field takes over maintenance of minimum inversion layer thickness at drain end.

- Larger gate-source bias $V_{GG}$ postpones flattening of $I_D$ vs $V_{DS}$ until larger values of drain current are reached.
MOSFET Switching Models for Buck Converter

- Buck converter using power MOSFET.

- MOSFET equivalent circuit valid for on-state (triode) region operation.

- MOSFET equivalent circuit valid for off-state (cutoff) and active region operation.
MOSFET Capacitances Determining Switching Speed

- Gate-source capacitance $C_{gs}$ approximately constant and independent of applied voltages.

- Gate-drain capacitance $C_{gd}$ varies with applied voltage. Variation due to growth of depletion layer thickness until inversion layer is formed.
Internal Capacitances Vs Spec Sheet Capacitances

MOSFET internal capacitances

Input capacitance

Reverse transfer or feedback capacitance

Bridge balanced ($V_b=0$) $C_{\text{bridge}} = C_{\text{gd}} = C_{\text{rss}}$

Output capacitance

$C_{\text{iss}} = C_{\text{gs}} + C_{\text{gd}}$

$C_{\text{oss}} = C_{\text{gd}} + C_{\text{ds}}$
Turn-on Equivalent Circuits for MOSFET Buck Converter

- Equivalent circuit during $t_{d(on)}$.

- Equivalent circuit during $t_{r_i}$.

- Equivalent circuit during $t_{fV1}$.

- Equivalent circuit during $t_{fV2}$.

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MOSFET-based Buck Converter Turn-on Waveforms

\[ V_{GS(th)} = R_G \left( C_{gd1} + C_{gs} \right) \]

\[ V_{GS(t)} = R_G \left( C_{gd2} + C_{gs} \right) \]

- Free-wheeling diode assumed to be ideal. (no reverse recovery current).
Turn-on Gate Charge Characteristic

\[ Q_{on} = \frac{1}{V_{gsoff}} \int [C_{gs}(V_{gs}) + C_{gd}(V_{gs})] V_{gs} dV_{gs} \]

\[ Q_p = \frac{1}{V_d} \int C_{gd}(V_{ds}) V_{ds} dV_{ds} \]

\[ Q_T = Q_{on} + Q_p + \frac{1}{V_{gs,off}} \int [C_{gs}(V_{gs}) + C_{gd}(V_{gs})] V_{gs} dV_{gs} \]

\[ (V_{t} + I_{D1}/g_m) \]

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Turn-on Waveforms with Non-ideal Free-wheeling Diode

- Equivalent circuit for estimating effect of free-wheeling diode reverse recovery.
MOSFET-based Buck Converter Turn-off Waveforms

• Assume ideal free-wheeling diode.

• Essentially the inverse of the turn-on process.

• Model quantitatively using the same equivalent circuits as for turn-on. Simply use correct driving voltages and initial conditions.
dV/dt Limits to Prevent Parasitic BJT Turn-on

- Turn-on of $T_+$ and reverse recovery of $D_{F-}$ will produce large positive $C_{gd} \frac{dV_{DS}}{dt}$ in bridge circuit.
- Parasitic BJT in $T_-$ likely to have been in reverse active mode when $D_{F-}$ was carrying current. Thus stored charge already in base which will increase likelihood of BJT turn-on when positive $C_{gd} \frac{dV_{DS}}{dt}$ is generated.

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Maximum Gate-Source Voltage

- \( V_{GS(\text{max})} \) = maximum permissible gate-source voltage.
- If \( V_{GS} > V_{GS(\text{max})} \) rupture of gate oxide by large electric fields possible.
- \( E_{BD(\text{oxide})} \approx 5-10 \text{ million V/cm} \)
  - Gate oxide typically 1000 angstroms thick
  - \( V_{GS(\text{max})} < [5 \times 10^6] [10^{-5}] = 50 \text{ V} \)
  - Typical \( V_{GS(\text{max})} 20 - 30 \text{ V} \)

- Static charge on gate conductor can rupture gate oxide
  - Handle MOSFETs with care (ground yourself before handling device)
  - Place anti-parallel connected Zener diodes between gate and source as a protective measure
MOSFET Breakdown Voltage

- \( BV_{DSS} \) = drain-source breakdown voltage with \( V_{GS} = 0 \)
- Caused by avalanche breakdown of drain-body junction
- Achieve large values by
  1. Avoidance of drain-source reach-through by heavy doping of body and light doping of drain drift region
  2. Appropriate length of drain drift region
  3. Field plate action of gate conductor overlap of drain region
  4. Prevent turn-on of parasitic BJT with body-source short (otherwise \( BV_{DSS} = BV_{CEO} \) instead of \( BV_{CBO} \))
• On-state power dissipation $P_{on} = I_o^2 r_{DS(on)}$

• Large $V_{GS}$ minimizes accumulation layer resistance and channel resistance

• $r_{DS(on)}$ dominated by drain drift resistance for $BV_{DSS} > \text{few 100 V}$

• $r_{DS(on)} = \frac{V_d}{I_D} \approx 3 \times 10^{-7} \frac{BV_{DSS}^2}{A}$

• $r_{DS(on)}$ increases as temperature increases. Due to decrease in carrier mobility with increasing temperature.
Paralleling of MOSFETs

- MOSFETs can be easily paralleled because of positive temperature coefficient of $r_{DS(on)}$.

- Positive temperature coefficient leads to thermal stabilization effect.

- If $r_{DS(on)}1 > r_{DS(on)}2$ then more current and thus higher power dissipation in $Q_2$.

- Temperature of $Q_2$ thus increases more than temperature of $Q_1$ and $r_{DS(on)}$ values become equalized.
MOSFET Safe Operating Area (SOA)

- No distinction between FBSOA and RBSOA. SOA is square.
  - FB = forward bias. $V_{GS} \geq 0$.
  - RB = reverse bias. $V_{GS} \leq 0$.
- No second breakdown.
Structural Comparison: VDMOS Versus COOLMOS™

- Conventional vertically oriented power MOSFET

- COOLMOS™ structure (composite buffer structure, super-junction MOSFET, super multi-resurf MOSFET)

- Vertical P and N regions of width b doped at same density (N_a = N_d)
**COOLMOS™ Operation in Blocking State**

- COOLMOS™ structure partially depleted.
- Arrows indicate direction of depletion layer growth as device turns off.
- Note n-type drift region and adjacent p-type stripes deplete uniformly along entire vertical length.

- COOLMOS™ structure at edge of full depletion with applied voltage $V_c$. Depletion layer reaches to middle of vertical P and N regions at $b/2$.
- Using step junction formalism, $V_c = (q b^2 N_d) / (4 \frac{d}{b}) = b E_{c,max}/2$
- Keep $E_{c,max} \leq E_{BD}/2$. Thus $N_d \leq \frac{E_{BD}}{(q b)}$
COOLMOS™ Operation in Blocking State (cont.)

- For applied voltages $V > V_c$, vertically oriented electric field $E_v$ begins to grow in depletion region.

- $E_v$ spatially uniform since space charge compensated for by $E_c$. $E_v \approx V/W$ for $V >> V_c$.

- Doping level $N_d$ in n-type drift region can be much greater than in drift region of conventional VDMOS drift region of similar $BV_{BD}$ capability.

- At breakdown $E_v = E_{BD} \approx 300 \text{ kV/cm} \ ; \ V = BV_{BD} = E_{BD}W$

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COOLMOS™ Operation in ON-State

- On-state specific resistance $R_{on} \, [\Omega \cdot \text{cm}^2]$ much less than comparable VDMOS because of higher drift region doping.

- COOLMOS™ conduction losses much less than comparable VDMOS.

- $R_{on} \, A = \frac{W}{(q \mu_n N_d)}$; Recall that $N_d = \frac{(E_{BD})}{(q b)}$

- Breakdown voltage requirements set $W = \frac{BV_{BD}}{E_{BD}}$.

- Substituting for $W$ and $N_d$ yields $R_{on} \, A = \frac{(b \cdot BV_{BD})}{(q \mu_n E_{BD}^2)}$
Ron A Comparison: VDMOS versus COOLMOS™

- COOLMOS at BV_{BD} = 1000 V. Assume b ≈ 10 µm. Use E_{BD} = 300 kV/cm.
  - R_{on} A = (10^{-3} \text{ cm}) (1000 \text{ V})/[ (9\times10^{-14} \text{ F/cm})(12)(1500 \text{ cm}^2 \cdot \text{V-sec})(300 \text{ kV/cm})^2]  
    R_{on} A = 0.014 \Omega \cdot \text{cm} . \text{Corresponds to } N_d = 4\times10^{15} \text{ cm}^{-3}

- Typical VDMOS,  R_{on} A = 3\times10^{-7} (BV_{BD})^2  
  - R_{on} A = 3\times10^{-7} (1000)^2 = 0.3 \Omega \cdot \text{cm} ; \text{Corresponding } N_d = 10^{14} \text{ cm}^3

- Ratio COOLMOS to VDMOS specific resistance = 0.007/0.3 = 0.023 or approximately 1/40
  - At BV_{BD} = 600 V, ratio = 1/26.
  - Experimentally at BV_{BD} = 600 V, ratio is 1/5.

COOLMOS™ Switching Behavior

- MOSFET switching waveforms for clamped inductive load.

- Larger blocking voltages $V_{ds} >$ depletion voltage $V_c$, COOLMOS has smaller $C_{gs}$, $C_{gd}$, and $C_{ds}$ than comparable (same $R_{on}$ and $BV_{DSS}$) VDMOS.

- Small blocking voltages $V_{ds} <$ depletion voltage $V_c$, COOLMOS has larger $C_{gs}$, $C_{gd}$, and $C_{ds}$ than comparable (same $R_{on}$ and $BV_{DSS}$) VDMOS.

- Effect on COOLMOS switching times relative to VDMOS switching times.
  - Turn-on delay time - shorter
  - Current rise time - shorter
  - Voltage fall time1 - shorter
  - Voltage fall time2 - longer
  - Turn-off delay time - longer
  - Voltage rise time1 - longer
  - Voltage rise time2 - shorter
  - Current fall time - shorter

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PSPICE Built-in MOSFET Model

Circuit components

- RG, RDS, RS, RB, and RD = parasitic ohmic resistances
- Cgs, Cgd, and Cgb = constant voltage-independent capacitors
- Cbs and Cbd = nonlinear voltage-dependent capacitors (depletion layer capacitances)
- Idrain = f(Vgs, Vds) accounts for dc characteristics of MOSFET
- Model developed for lateral (signal level) MOSFETs
Lateral (Signal level) MOSFET

- Body-source short keeps $C_{bs}$ constant.

- Body-source short puts $C_{bd}$ between drain and source.

- Variations in drain-source voltage relatively small, so changes in $C_{bd}$ also relatively small.

- Capacitances relatively independent of terminal voltages

- Consequently PSPICE MOSFET model has voltage-independent capacitances.

- $C_{gs}$, $C_{bg}$, $C_{gd}$ due to electrostatic capacitance of gate oxide. Independent of applied voltage.

- $C_{bs}$ and $C_{bd}$ due to depletion layers. Capacitance varies with junction voltage.

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Vertical Power MOSFET

- Drain-drift region and large drain-source voltage variations cause large variations in drain-body depletion layer thickness.
  - Large changes in $C_{gd}$ with changes in drain-source voltage. 10 to 100:1 changes in $C_{gd}$ measured in high voltage MOSFETs.
  - Moderate changes in $C_{gb}$ and $C_{bs}$.

- MOSFET circuit simulation models must take this variation into account.

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Inadequacies of PSPICE MOSFET Model

- $C_{gs}$ and $C_{gd}$ in PSPICE model are constant independent of terminal voltages.

- In vertical power MOSFETs, $C_{gd}$ varies substantially with terminal voltages.

- Comparison of transient response of drain-source voltage using PSPICE model and an improved subcircuit model. Both models used in same step-down converter circuit.
Example of an Improved MOSFET Model

- Developed by Motorola for their TMOS line of power MOSFETs
- M1 uses built-in PSPICE models to describe dc MOSFET characteristics. Space charge capacitances of intrinsic model set to zero.
- Space charge capacitance of DGD models voltage-dependent gate-drain capacitance.
- CGDMAX insures that gate-drain capacitance does not get unrealistically large at very low drain voltages.
- DBODY models built-in anti-parallel diode inherent in the MOSFET structure.
- CGS models gate-source capacitance of MOSFET. Voltage dependence of this capacitance ignored in this model.
- Resistances and inductances model parasitic components due to packaging.
- Many other models described in literature. Too numerous to list here.
Another Improved MOSFET Simulation Model

- M2 and M3 are SPICE level 2 MOSFETs used along with $V_{\text{offset}}$ to model voltage dependent behavior of $C_{\text{gd}}$.
- JFET $Q_1$ and $R_d$ account for voltage drop in $N^-$ drain drift region.
- $D_{\text{sub}}$ is built-in SPICE diode model used to account for parasitic anti-parallel diode in MOSFET structure.

- M1= intrinsic SPICE level 2 MOSFET with no parasitic resistances or capacitances.

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Lecture Notes

Thyristors (SCRs)

OUTLINE

- SCR construction and I-V characteristics.
- Physical operation of SCRs.
- Switching behavior of SCRs
- $dv/dt$ and $di/dt$ limitations and methods of improving them.
- SCR drive circuit considerations.
Thyristor (SCR) Geometry

Gate and cathode metallization for slow (phase control) thyristor.

Gate and cathode metallization for fast (inverter grade) SCR

• Cross-sectional view showing vertical orientation of SCR.
• SCR with kiloamp ratings have diameters of 10 cm or greater.
• SCR triggerable from forward blocking state to on-state by a gate current pulse.

• Thyristor latches on and gate cannot turn it off. External circuit must force SCR off.

• Current to several kiloamps for $V(\text{on})$ of 2-4 volts.

• Blocking voltages to 5-8 kilovolts.

• $V_{BO} = \text{breakover voltage} ; I_{BO} = \text{breakover current}$

• $V_H = \text{holding voltage} I_H = \text{holding current}$

• Maximum junction temperature = 125 °C - limited by temperature dependence of $V_{BO}$. 
SCR Model and Equivalent Circuit

One dimensional SCR model.

- BJTs in equivalent circuit in active region.
- Use Ebers-Moll equations for BJTs
  - $I_{C1} = -a_1 I_E1 + I_{C01}$ ; $I_{C2} = -a_2 I_E2 + I_{C0}$
  - $I_A = I_E1$ ; $I_K = -I_E2 = I_A + I_G$
  - $I_{C1} + I_{B1} + I_E1 = 0$
  - $I_A = \frac{I_G + I_{C01} + I_{C02}}{1 - a_1 - a_2}$
- Blocking state $a_1 + a_2 << 1$
- At breakover $a_1 + a_2 \approx 1$

Two transistor equivalent circuit
Thyristor Turn-on Process

- In forward blocking state, both BJTs active.
- If $\alpha_1 + \alpha_2 < 1$, connection is stable.
- If $V_{AK} = V_{BO}$ or if positive gate current pulse is applied $\alpha_1 + \alpha_2$ becomes equal to unity and circuit connection becomes unstable and SCR switches on.

- Negative charge of electrons swept into $n_1$ layer partially compensate positive charge of ionized donors exposed by growth of depletion of junction $J_2$.

- Growth of depletion reduces width of bases of $Q_{npn}$ and $Q_{pnp}$ and thus increases $\alpha_1$ and $\alpha_2$.

- Holes attracted by first wave of injected electrons attract additional electrons and so on - regenerative action.
Thyristor On-state Latchup

- Negative gate current causes lateral voltage drops as indicated which lead to current crowding in center of cathode.

- Conventional SCRs (phase control) have large area cathodes - negative gate current cannot remove stored charge from center of large cathode area.

- SCR stays latched on in spite of negative gate current.

- External circuit must force anode current to negative values in order that enough stored charge be removed from SCR so that it can turn off.
Thyristor On-state Operation

- On-state: all three junctions forward biased and BJTs in equivalent circuit saturated.

- On-state stable because saturated BJTs have $a_1 + a_2 << 1$.

- On-state voltage $V_{AK(on)} = V_{j1} - V_{j2} + V_{j3} + V_n$
Thyristor Turn-on Behavior

- \( t_{d(on)} \) = turn-on delay time; time required for charge injection by gate current to make \( \square_1 + \square_2 = 1 \).

- \( t_r \) = time required for anode current to reach on-state value. Anode current rate-of-rise \( \frac{di_F}{dt} \) limited by external inductance.

- \( t_{ps} \) = time required for plasma to spread over whole cathode area from cathode periphery near gate.

- \( V_{AK} \) does not attain on-state value until complete area of cathode is conducting.
Thyristor Turn-off Behavior

- SCR turn-off quite similar to power diode turn-off.
- Anode current rate-of-fall controlled by external inductance.
- Reverse voltage overshoot caused by external inductance.
- Junction J₁ is blocking junction in reverse bias. J₃ has low breakdown voltage (20-40 volts) because of the heavy doping on both sides of the junction.
Thyristor di/dt Limit at Turn-on

- SCR first turns on at cathode periphery nearest gate.

- Current constricted to small areas during initial phases of turn-on, $t_{d(on)}$ and $t_r$.

- If anode current rate-of-rise, $di_F/dt$, not kept less than some specified maximum, current density in constricted area will be too large.

- Localized power dissipation too high and thermal runaway likely.

- Use shaped gate current pulse for rapid turn-on.
Thyristor Re-applied \(dv/dt\) Limits

- Removal of all stored charge in SCR requires a minimum time \(t_q\).
- Application of positive \(dV_F/dt\) larger than a specified value before \(t_q\) results in a pulse of positive anode current which may produce unintentioned turn-on of the SCR.
- Avoidance of unintentioned turn-on requires \(dV_F/dt < dV_{F,\text{max}}/dt\) and remaining in reverse bias for a minimum time \(t_q\).

\[
\frac{dv_F}{dt} \bigg|_{\text{max}} < \frac{I_{BO}}{C_{j2}}
\]

Rate effect

\[
100 \text{ V/s} < \frac{dv_F}{dt} \bigg|_{\text{max}} < 2000 \text{ V/s}
\]
Methods of Improving Thyristor $\frac{di}{dt}$ Rating

- Interdigitated gate-cathode structure used to greatly increase gate-cathode periphery.

- Distance from periphery to center of any cathode region significantly shortened.

- Ability of negative gate current to break latching condition in on-state increased.

- Combination of pilot thyristor, diode, and interdigitated gate-cathode geometry termed a gate-assisted turn-off thyristor or GATT.

- Use of pilot thyristor to increase turn-on gate current to main thyristor.

- Larger gate current increases amount of initial conducting area of cathode and thus improves $\frac{di}{dt}$ capabilities.

- Diode allows negative gate current to flow from main SCR.
Improvement in $\frac{dv}{dt}$ Rating Via Cathode Shorts

- Current thru $C_{j2}$ indistinguishable from positive gate current with respect to turn-on of SCR.
- If current thru $C_{j2}$ bypasses junction $J_3$, then SCR will not be turned on by the large displacement currents.
- Cathode shorts provide this desirable bypass. Most effective with interdigitated gate-cathode geometry.

\[ \frac{dV_F}{dt} \text{ significantly increased.} \]
Thyristor Gate Trigger Requirements

Equivalent circuit of SCR drive circuit

Gate current must be on for a specified minimum time interval (few tens of microseconds) to guarantee SCR turn-on
Lecture Notes

Gate Turn-off Thyristors (GTOS)

OUTLINE

• GTO construction and I-V characteristics.
• Physical operation of GTOs.
• Switching behavior of GTOS
GTO (Gate Turn-off Thyristor) Construction

- Unique features of the GTO.
  - Highly interdigitated gate-cathode structure (faster switching)
  - Etched cathode islands (simplify electrical contacts)
  - Anode shorts (speed up turn-off)
  - GTO has no reverse blocking capability because of anode shorts
- Otherwise i-v characteristic the same as for standard SCR

GTO circuit symbol
**GTO Turn-off Gain**

- Turn off GTO by pulling one or both of the BJTs out of saturation and into active region.
- Force Q2 active by using negative base current $I_G'$ to make $I_{B2} < \frac{I_{C2}}{\Delta 2}$

$$I_{B2} = \Delta 1 I_A - I_G' \quad ; \quad I_{C2} = (1 - \Delta 1) I_A$$

$$\Delta 1 I_A - I_G' < \frac{(1 - \Delta 1) I_A}{\Delta 2} = \frac{(1 - \Delta 1)(1 - \Delta 2) I_A}{\Delta 2}$$

$$I_G' < \frac{I_A}{\Delta_{off}} \quad ; \quad \Delta_{off} = \frac{\Delta 2}{(1 - \Delta 1 - \Delta 2)} = \text{turn-off gain}$$

- Large turn-off gain requires $\Delta 2 \approx 1, \Delta 1 << 1$

- Make $\Delta 1$ small by
  1. Wide $n_1$ region (base of Q1) - also needed for large blocking voltage
  2. Short lifetime in $n_1$ region to remove excess carriers rapidly so Q1 can turn off

- Short lifetime causes higher on-state losses

- Anode shorts helps resolve lifetime delimma
  1. Reduce lifetime only moderately to keep on-state losses reasonable
  2. N$^+$ anode regions provide a sink for excess holes - reduces turn-off time

- Make $\Delta 2 \approx$ unity by making p$_2$ layer relatively thin and doping in n$_2$ region heavily (same basic steps used in making beta large in BJTs).

- Use highly interdigitated gate-cathode geometry to minimize cathode current crowding and di/dt limitations.

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Maximum Controllable Anode Current

- Large negative gate current creates lateral voltage drops which must be kept smaller than breakdown voltage of J₃.

- If J₃ breaks down, it will happen at gate-cathode periphery and all gate current will flow there and not sweep out any excess carriers as required to turn-off GTO.

- Thus keep gate current less than I_{G,max} and so anode current restricted by \( I_A < \frac{I_{G,max}}{\Delta \text{off}} \)
GTO used in medium-to-high power applications where electrical stresses are large and where other solid state devices used with GTOs are slow e.g. free-wheeling diode $D_F$.

GTO almost always used with turn-on and turn-off snubbers.

1. Turn-on snubber to limit overcurrent from $D_F$ reverse recovery.

2. Turn-off snubber to limit rate-of-rise of voltage to avoid retriggering the GTO into the on-state.

Hence should describe transient behavior of GTO in circuit with snubbers.
GTO turn on essentially the same as for a standard thyristor

Large $I_{GM}$ and large rate-of-rise insure all cathode islands turn on together and have good current sharing.

Backporch current $I_{GT}$ needed to insure all cathode islands stay in conduction during entire on-time interval.

Anode current overshoot caused by free-wheeling diode reverse recovery current.

Anode-cathode voltage drops precipitiously because of turn-on snubber.
GTO Turn-off Waveforms

• $t_s$ interval
  Time required to remove sufficient stored charge to bring BJTs into active region and break latch condition

• $t_f$ interval
  1. Anode current falls rapidly as load current commutates to turn-off snubber capacitor
  2. Rapid rise in anode-cathode voltage due to stray inductance in turn-off snubber circuit

• $t_{w2}$ interval
  1. Junction $J_3$ goes into avalanche breakdown because of inductance in trigger circuit. Permits negative gate current to continuing flowing and sweeping out charge from $p_2$ layer.
  2. Reduction in gate current with time means rate of anode current commutation to snubber capacitor slows. Start of anode current tail.

• $t_{tail}$ interval
  1. Junction $J_3$ blocking, so anode current = negative gate current. Long tailing time required to remove remaining stored charge.
  2. Anode-cathode voltage growth governed by turn-off snubber.
  3. Most power dissipation occurs during tailing time.
Lecture Notes

Insulated Gate Bipolar Transistors (IGBTs)

Outline

- Construction and I-V characteristics
- Physical operation
- Switching characteristics
- Limitations and safe operating area
- PSPICE simulation models
IGBT = insulated gate bipolar transistor.
Cross-section of IGBT Cell

- Cell structure similar to power MOSFET (VDMOS) cell.
- P-region at collector end unique feature of IGBT compared to MOSFET.
- Punch-through (PT) IGBT - N⁺ buffer layer present.
- Non-punch-through (NPT) IGBT - N⁺ buffer layer absent.
Cross-section of Trench-Gate IGBT Unit Cell

- Non-punch-thru IGBT
- Punch-thru IGBT
IGBT I-V Characteristics and Circuit Symbols

- No Buffer Layer
  \( V_{RM} \approx BV_{CES} \)
- With Buffer Layer
  \( V_{RM} \approx 0 \)

- N-channel IGBT circuit symbols

\[ \begin{align*}
  & V_{GE} \\
  & BV_{CES} \\
  & i_C \\
  & v_C \\
  & v_{GE1} \\
  & v_{GE2} \\
  & v_{GE3} \\
  & v_{GE4} \\
  & V_{GE(th)} \\
\end{align*} \]
Blocking (Off) State Operation of IGBT

- Blocking state operation - $V_{GE} < V_{GE(th)}$
- Junction $J_2$ is blocking junction - $n^+$ drift region holds depletion layer of blocking junction.
- Without $N^+$ buffer layer, IGBT has large reverse blocking capability - so-called symmetric IGBT
- With $N^+$ buffer layer, junction $J_1$ has small breakdown voltage and thus IGBT has little reverse blocking capability - anti-symmetric IGBT
- Buffer layer speeds up device turn-off

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IGBT On-state Operation

- MOSFET section designed to carry most of the IGBT collector current
- On-state $V_{CE(on)} = V_{J1} + V_{\text{drift}} + I_{CR\text{channel}}$
- Hole injection into drift region from $J_1$ minimizes $V_{\text{drift}}$. 

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Approximate Equivalent Circuits for IGBTs

• Approximate equivalent circuit for IGBT valid for normal operating conditions.

\[ V_{CE(on)} = V_{J1} + V_{drift} + I_{C} R_{channel} \]

• IGBT equivalent circuit showing transistors comprising the parasitic thyristor.
Static Latchup of IGBTs

Conduction paths causing lateral voltage drops and turn-on of parasitic thyristor if current in this path is too large

- Lateral voltage drops, if too large, will forward bias junction J3.
- Parasitic npn BJT will be turned on, thus completing turn-on of parasitic thyristor.
- Large power dissipation in latchup will destroy IGBT unless terminated quickly. External circuit must terminate latchup - no gate control in latchup.
Dynamic Latchup Mechanism in IGBTs

- MOSFET section turns off rapidly and depletion layer of junction J2 expands rapidly into N⁻ layer, the base region of the pnp BJT.
- Expansion of depletion layer reduces base width of pnp BJT and its a increases.
- More injected holes survive traversal of drift region and become “collected” at junction J2.
- Increased pnp BJT collector current increases lateral voltage drop in p-base of npn BJT and latchup soon occurs.
- Manufacturers usually specify maximum allowable drain current on basis of dynamic latchup.
Internal Capacitances Vs Spec Sheet Capacitances

\[ C_{gc} \]

\[ C_{ge} \]

\[ C_{ce} \]

\[ C_{ies} \]

\[ C_{res} \]

Bridge balanced (Vb=0) \( C_{bridge} = C_{gc} = C_{res} \)

\[ C_{oes} \]

\[ C_{gc} \]

\[ C_{ce} \]
• Turn-on waveforms for IGBT embedded in a stepdown converter.

• Very similar to turn-on waveforms of MOSFETs.

• Contributions to $t_{vf2}$.

  • Increase in $C_{ge}$ of MOSFET section at low collector-emitter voltages.

  • Slower turn-on of pnp BJT section.
IGBT Turn-off Waveforms

- Turn-off waveforms for IGBT embedded in a stepdown converter.

- Current “tailing” (t_{fi2}) due to stored charge trapped in drift region (base of pnp BJT) by rapid turn-off of MOSFET section.

- Shorten tailing interval by either reducing carrier lifetime or by putting N^+ buffer layer adjacent to injecting P^+ layer at drain.

- Buffer layer acts as a sink for excess holes otherwise trapped in drift region because lifetime in buffer layer can be made small without effecting on-state losses - buffer layer thin compared to drift region.
IGBT Safe Operating Area

- Maximum collector-emitter voltages set by breakdown voltage of pnp transistor - 2500 v devices available.

- Maximum collector current set by latchup considerations - 100 A devices can conduct 1000 A for 10 µsec and still turn-off via gate control.

- Maximum junction temp. = 150 C.

- Manufacturer specifies a maximum rate of increase of re-applied collector-emitter voltage in order to avoid latchup.
Development of PSpice IGBT Model

- Nonlinear capacitors Cdsj and Ccer due to N-P junction depletion layer.
- Nonlinear capacitor Cebj + Cebd due to P+N+ junction
- MOSFET and PNP BJT are intrinsic (no parasitics) devices
- Nonlinear resistor Rb due to conductivity modulation of N- drain drift region of MOSFET portion.
- Nonlinear capacitor Cgdj due to depletion region of drain-body junction (N-P junction).
- Circuit model assumes that latchup does not occur and parasitic thyristor does not turn.

Parameter Estimation for PSpice IGBT Model

• Built-in IGBT model requires nine parameter values.
  • Parameters described in Help files of Parts utility program.

• Parts utility program guides users through parameter estimation process.
  • IGBT specification sheets provided by manufacturer provide sufficient information for general purpose simulations.
  • Detailed accurate simulations, for example device dissipation studies, may require the user to carefully characterize the selected IGBTs.

• Built-in model does not model ultrafast IGBTs with buffer layers (punch-through IGBTs) or reverse free-wheeling diodes.
PSpice IGBT - Simulation Vs Experiment

Data from IXGH40N60 spec sheet
Simulated \( C_{GC} \) versus \( V_{CE} \) for IXGH40N60
\( V_{GE} = 0 \) V

Collector - emitter Voltage
Lecture Notes

Emerging Devices

Outline

• Power JFET Devices
• Field-Controlled Thyristor
• MOS-Controlled Thyristor
• High Voltage Integrated Circuits/ Discrete Modules
• New Semiconductor Materials
Power JFET Geometry

- Gate-source geometry highly interdigitated as in MOSFETs.
- Width \( w = \mu \text{ms} \) to a few tens of \( \mu \text{ms} \); \( l_c < w \); \( l_{gs} \) minimized.
- \( l_{gd} \) set by blocking voltage considerations.
Power JFET I-V Characteristics

- Power JFET is a normally-on device. Substantial current flows when gate-source voltage is equal to zero.
- Opposite to BJTs, MOSFETs, and IGBTs which are normally-off devices.
Controlling Potential Barrier in JFETs

- $|V_{GS}| > |V_p|$ (pinchoff voltage) potential barrier to electron flow from source to drain created. No drain current can flow.

- Suppress potential barrier by increasing $V_{DS}$ at fixed $V_{GS}$. When $V_{DS} > \mu |V_{GS}|$ substantial drain currents flow.

- Blocking capability limited by magnitude of electric field in drift region. Longer drift regions have larger blocking voltage capability.

- Normally-off JFET created by having narrow enough channel width so that the channel is pinched off at zero gate-source voltage.
JFET On and Off States

- **JFET in on-state**
  - Channel open between drain and source.

- **JFET in blocking state**
  - Channel pinched-off (closed) between drain and source.
Bipolar Static Induction Transistor (BSIT)

BSIT in blocking state

- Channel width and channel doping chosen so that at zero gate-source voltage, depletion layers of gate-channel junction pinch-off the channel.
- Narrower channel than normally-on JFET.

JFET in on-state

- Forward bias gate-channel junction to reduce depletion region width and open up channel.
- Substantial current flow into gate.
JFET Switching Characteristics

- Equivalent circuits of JFETs nearly identical to those of MOSFETs.

- Switching waveforms nearly identical to those of MOSFETs including values of various switching time intervals.

- JFET $V_{GS}$ starts at negative values and steps to zero at turn-on while MOSFET $V_{GS}$ starts at zero and steps to positive value at turn-on.

- FET on-state losses somewhat higher than for MOSFET - technology related not fundamental.

- Normally-off JFET (Bipolar static induction transistor or BSIT) switching characteristics more similar to those of BJT.

- Differences between BSIT and BJT observable mainly at turn-off.
  
  1. BSIT has no quasi-saturation region and thus only one current fall time (no current tailing) at turn-off.

  2. Overall turn-off times of BSIT shorter than for BJT.

  3. Differences due to fact that BSIT has no in-line pn junction that can block sweep-out of excess carriers as does BJT.
Field-Controlled Thyristor (FCT)

Vertical Cross-section

Injecting contact - unique feature of FCT

• Sometimes termed a bipolar static induction thyristor (BSIThy).

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FCT I-V Characteristics

- FCT has a normally-on characteristic.
- Can be made to have a normally-off characteristic.

1. Reduce channel width so that zero-bias depletion layer width of gate-channel junction pinches off channel

2. Then termed a bipolar static induction thyristor (BSIThy).
Physical Operation of FCT

- FCT essentially a power JFET with an injecting contact at the drain.

- Injecting contact causes conductivity modulation of drain drift region and results in much lower on-state losses.

- At turn-off, gate draws large negative current similar to a GTO because of stored charge in drift region.

- FCT not a latching switch as is a GTO. FCT has no regenerative action.

- FCT can be made a normally-off device by using narrow channel widths so that zero-bias width gate depletion layer pinches off channel.

- Cascode switching circuit.

- Implement a normally-off composite switch.

- R1 and R2 insure that voltage across MOSFET not overly large. Permits use of low voltage-high current device.

![Diagram of FCT circuit](image-url)
FCT Switching Characteristics

- FCT switching waveforms qualitatively similar to thyristor or GTO including large negative gate current at turn-off.

- FCT has gate-controlled turn-on and turn-off capabilities similar to GTO.

- FCT switching times somewhat shorter than GTO.

- Gate drive must be continuously applied to FCT because FCT has no latching characteristic.

- FCT has much larger re-applied dv/dt rating than GTO because of lack of latching action.

- FCT has di/dt limits because of localized turn-on and then expansion of turned-on region across entire device cross-section.
JFET-Based Devices Vs Other Power Devices

- Blocking voltage capability of JFETs comparable to BJTs and MOSFETs.

- JFET on-state losses higher than MOSFETs - technology limitation.

- Switching speeds of normally-on JFET somewhat slower than those of MOSFET - technology limitation.

- BSIT switching times comparable to BJTs - in principle should be faster because of lack of in-line pn junction trapping stored charge at turn-off.

- No second breakdown in normally-on JFETs, similar to MOSFETs.

- BSITs and BSITHy have and possibly limitations.

- JFET-based power devices much less widely used because of normally-on characteristic. This has also slowed research and development efforts in these devices compared to other devices.
P-MCT (P-type MOS-controlled Thyristor)

Unit cell vertical cross-section

- Complete MCT composed of tens of thousands of identical cells connected in parallel.

- P-designation refers to doping of the lightly-doped P⁺ layer which contains the depletion layer of the blocking junction.

- Note that ON and OFF FETs are positioned at the anode end of the device.
P-MCT Equivalent Circuit & Circuit Symbol

- P-MCT used with anode grounded.
- Gate-anode voltage is input drive voltage.
- Use P-MCT in circuits with negative voltages.
N-MCT (N-type MOS-controlled Thyristor)

Vertical cross-section of N-MCT unit cell

- N-MCT composed of thousands of cells connected electrically in parallel.
- N-designation refers to the N⁻ layer which contains the depletion layer of the blocking junction.
- Note that the ON and OFF FETs are positioned at the cathode end of the device.
N-MCT Equivalent Circuit & Circuit Symbol

- N-MCT used with cathode grounded.
- Gate-cathode voltage is input drive voltage.
- Use N-MCT in circuits with positive voltages.
Gate-controlled Turn-on of MCTs

• Turn on MCT by turning on the ON-FET
  • Positive gate-cathode voltage for N-MCT
  • Negative gate-anode voltage for P-MCT
  • These polarities of gate voltage automatically keep the OFF-FET in cutoff.

• ON-FET delivers base current to the low-gain BJT in the thyristor equivalent circuit and activates that BJT.
  • PNP transistor in the N-MCT
  • NPN transistor in the P-MCT

• Low-gain transistor activates the higher gain transistor and thyristor latches on.

• Once higher gain transistor, which is in parallel with ON-FET is activated, current is shunted from ON-FET to the BJT and the ON-FET carries very little current in the MCT on-state.
  • Only 5-10% of the cells have an ON-FET.
  • Cells are close-packed. Within one excess carrier diffusion length of each other.
  • Adjacent cells without an ON-FET turned on via diffusion of excess carriers from turned-on cell.
Gate-controlled Turn-off of MCTs

- Turn MCT off by turning on the OFF-FET
  - Negative gate-cathode for the N-MCT
  - Positive gate-anode voltage for the P-MCT
  - These gate voltage polarities automatically keep the ON-FET in cut-off.

- OFF-FET shunts base current away from the higher gain BJT in the thyristor equivalent circuit and forces it to cut-off.
  - NPN transistor in the N-MCT.
  - PNP transistor in the P-MCT.

- Cut-off of higher gain BJT then forces low-gain BJT into cut-off.

- Every MCT cell has an OFF-FET.

- OFF-FET kept activated during entire MCT off-state to insure no inadvertent activation of the thyristor.
Maximum Controllable Anode Current

- If drain-source voltage of OFF-FET reaches approximately 0.7 V during turn-off, then MCT may remain latched in on-state.

- Higher-gain BJT remains on if OFF-FET voltage drop, which is the base-emitter voltage of the BJT reaches 0.7 volts.

- Thus maximum on-state current that can be turned off by means of gate control.

- P-MCT have approximately three times larger gate-controlled anode current rating than a similar (same size and voltage rating) N-MCT.

- OFF-FET of the P-MCT is an n-channel MOSFET which has three times larger channel mobility than the p-channel OFF-FET of the N-MCT.
Rationale of OFF-FET Placement

- Turning off the BJT with the larger value of $a$ is the most effective way to break the latching condition

$$a_1 + a_2 = 1$$

- BJT with the smaller base width has the larger value of $a$.
  - P-MCT; PNP BJT has smaller base width
  - N-MCT; NPN BJT has smaller base width

- OFF-FET put in parallel with base-emitter of larger gain BJT so that OFF-FET shorts out base-emitter when the FET is activated.
MCT Switching Waveforms

N-MCT Step-down Converter

P-MCT Step-down Converter

Emerging Devices - 21
MCT Turn-on Process

- Turn-on delay time $t_{d,on}$ - time required for gate voltage to reach ON-FET threshold starting from reverse-bias value of $V_{GG,off}$

- Current rise time $t_{ri1}$ and $t_{ri2}$
  - $t_{ri1}$: ON-FET turns on accepting all the current the gate drive voltage will permit. ON-FET in its active region.
  - $t_{ri2}$: NPN and PNP BJTs turn on and current shunted away from ON-FET. BJTs and ON-FET in their active regions.

- Voltage fall time $t_{fv1}$ and $t_{fv2}$
  - $t_{fv1}$: BJTs in their active regions so voltage fall initially fast.
  - $t_{fv2}$: BJTs in quasi-saturation, so their gain is reduced and rate of voltage fall decreases.
  - At end of voltage fall time interval, BJTs enter hard saturation and MCT is in the on-state.

- Gate-cathode voltage should reach final on-state value in times no longer than a specified maximum value (typically 200 nsec). Insure that all paralleled cells turn on at the same time to minimize current crowding problems.

- Keep gate-cathode at on-state value for the duration of the on-state to minimize likelihood of inadvertant turn-off of some cells if current is substantially reduced during on-state.
MCT Turn-off Process

• Turn-off delay time $t_{d, \text{off}}$ - time required to turn-off the ON-FET, activate the OFF-FET, and break the latching condition by pulling the BJTs out of hard saturation and into quasi-saturation.
  • Requires removal of substantial amount of stored charge, especially in the base regions of the two BJTs ($n_1$ and $p_2$ thyristor layers).

• Voltage rise times $t_{rv1}$ and $t_{rv2}$
  • $t_{rv1}$: time required to remove sufficient stored charge so that BJTs leave quasi-saturation and enter active region and blocking junction ($J_2$) becomes reverse-biased.
  • $t_{rv2}$: BJTs in active region and their larger gain causes anode voltage to rapidly complete growth to power supply voltage $V_d$

• Current fall time $t_{fi1}$ and $t_{fi2}$
  • $t_{fi1}$: Initial rapid fall in current until high gain BJT (NPN BJT in the P-MCT equivalent circuit) goes into cutoff.
  • $t_{fi2}$: stored charge still remaining in base (drift region of thyristor) of the low-gain BJT removed in this interval. The open-base nature of the turn-off causes longer time interval giving a "tail" to the anode current decay.

• Gate-cathode voltage kept at off-state value during entire off-state interval to prevent accidental turn-on.
MCT Operating Limitations

- $I_{\text{max}}$ set by maximum controllable anode current. Presently available devices have 50-100 A ratings.

- $V_{\text{max}}$ set by either breakover voltage of thyristor section or breakdown rating of the OFF-FET. Presently available devices rated at 600 V. 1000-2000 V devices prototyped.

- $\frac{dv_{DS}}{dt}$ limited by mechanisms identical to those in thyristors. Presently available devices rated at 500-1000 V/sec.

- $\frac{di_D}{dt}$ limited by potential current crowding problems. Presently available devices rated at 500 A/sec.

- MCT safe operating area. Very conservatively estimated.
High Voltage (Power) Integrated Circuits

- Three classes of power ICs
  
  1. Smart power or smart/intelligent switches
     - Vertical power devices with on-chip sense and protective features and possibly drive and control circuits
  
  2. High voltage integrated circuits (HVICs)
     - Conventional ICs using low voltage devices for control and drive circuits and lateral high voltage power devices
  
  3. Discrete modules
     - Multiple chips mounted on a common substrate. Separate chips for drive, control, and power switch and possibly other functions.

- PIC rationale
  
  - Lower costs
  
  - Increased functionality
  
  - Higher reliability
  
  - Less circuit/system complexity
Issues Facing PIC Commercialization

- Technical issues
  - Electrical isolation of high voltage devices from low voltage components
  - Thermal management - power devices generally operate at higher temperatures than low power devices/circuits.
  - On-chip interconnections with HV conductor runs over low voltage devices/regions.
  - Fabrication process should provide full range of devices and components - BJT\textsuperscript{s}, MOSFET\textsuperscript{s}, diodes, resistors, capacitors, etc.

- Economic issues
  - High up-front development costs
  - Relative cost of the three classes of PIC\textsuperscript{s}
  - Need for high volume applications to cover development expenses.
Dielectric Isolation

- Dielectrically isolated tubs - SiO₂ isolation and silicon thin film overgrowth.

- Wafer bonding and subsequent wafer thinning.
Self-Isolation and Junction Isolation

- Self-isolation - only feasible with MOSFET devices.

- Junction isolation.
High-Voltage Low-Voltage Cross-overs

- Field-crowding and premature breakdown.

- Use of field shields to minimize field crowding problems at HV/LV cross-overs.
Smart or Intelligent Switch Using MOSFETs

- Cross-sectional diagram of switch.

- Add additional components on vertical MOSFET wafer as long as no major process changes required.

- PN junction formed from $N^-$ drift region and P-body region always reverse-biased if drain of power MOSFET positive respect to source. Provides electrical isolation of the two MOSFETs.
**Smart Power Switch Using BJTs**

Cross-sectional view

- Three electrically isolated BJTs diagramed
  - PN junction isolation via P-epi and top-side P+ diffusion

- Double epitaxial process sequence
  - P-epi grown on N+ substrate
  - N+ buried layer diffused in next
  - N-epi for drift region grown over P-epi
  - P+ isolation diffusions to P-epi
  - Diffusion for base and emitters of BJTs
High Voltage Integrated Circuits (HVICs)

Lateral HV DMOSFET
Lateral Logic Level NPN BJT
Lateral Logic Level PNP BJT

P-substrate

HVIC using junction isolation

Lateral HV N-channel DMOSFET
Lateral Logic Level N-MOSFET
Lateral Logic Level P-MOSFET

P^- substrate

HVIC using self-isolation
Discrete Module Example - IXYS I³M IGBT Module

- Intelligent isolated half-bridge
- 200 A - 1080 V
- Built-in protection and sensing of overcurrents, overvoltages, overtemperatures, short circuits.
- Modules with only IGBTs and anti-parallel diodes available with ratings of 3300V - 1200A
IGCT - Integrated Gate Commutated Thyristor

- Specially designed GTO with low inductance gate drive circuit
- Ratings
  - Blocking voltage - 4500V
  - Controllable on-state current - 4000A
  - Average fwd current - 1200A
  - Switching times - 10µsec

- Approximate gate drive circuit
  - Ion ≈ 500 A 10µsec
  - Ioff - full forward current 10 usec
  - Very low series inductance - 3 nH
Emitter Turn-off Thyristor

- Performance similar to IGCTs
- Advantages over IGCTs
  - Simpler drive circuit
  - Easier to parallel - MOSFETs in series with GTO have positive temperature coefficient
  - Series MOSFETs can be used for overcurrent sensing
Economic Considerations in PIC Availability

- PIC development costs (exclusive of production costs)
  - Discrete modules have lower development costs
  - Larger development costs for smart switches and HVICs

- Production costs (exclusive of development costs) of smart switches and HVICs lower than for discrete modules.

- Reliability of smart switches and HVICs better than discrete modules.
  - Greater flexibility/functionality in discrete modules
  - Wider range of components - magnetics, optocouplers

- PICs will be developed for high volume applications
  - Automotive electronics
  - Telecommunications
  - Power supplies
  - Office automation equipment
  - Motor drives
  - Fluorescent lighting ballasts
New Semiconductor Materials for Power Devices

- Silicon not optimum material for power devices

- Gallium arsenide promising material
  - Higher electron mobilities (factor of about 5-6) - faster switching speeds and lower on-state losses
  - Larger band-gap $E_g$ - higher operating temperatures

- Silicon carbide another promising materials
  - Larger bandgap than silicon or GaAs
  - Mobilities comparable to Si
  - Significantly larger breakdown field strength
  - Larger thermal conductivity than Si or GaAs

- Diamond potentially the best materials for power devices
  - Largest bandgap
  - Largest breakdown field strength
  - Largest thermal conductivity
  - Larger mobilities than silicon but less than GaAs
## Properties of Important Semiconductor Materials

<table>
<thead>
<tr>
<th>Property</th>
<th>Si</th>
<th>GaAs</th>
<th>3C-SiC</th>
<th>6H-SiC</th>
<th>Diamond</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Bandgap @ 300 °K [eV]</strong></td>
<td>1.12</td>
<td>1.43</td>
<td>2.2</td>
<td>2.9</td>
<td>5.5</td>
</tr>
<tr>
<td><strong>Relative dielectric constant</strong></td>
<td>11.8</td>
<td>12.8</td>
<td>9.7</td>
<td>10</td>
<td>5.5</td>
</tr>
<tr>
<td><strong>Saturated drift velocity [cm/sec]</strong></td>
<td>$1 \times 10^7$</td>
<td>$2 \times 10^7$</td>
<td>$2.5 \times 10^7$</td>
<td>$2.5 \times 10^7$</td>
<td>$2.7 \times 10^7$</td>
</tr>
<tr>
<td><strong>Thermal conductivity [Watts/cm-°C]</strong></td>
<td>1.5</td>
<td>0.5</td>
<td>5.0</td>
<td>5.0</td>
<td>20</td>
</tr>
<tr>
<td><strong>Maximum operating temperature [°K]</strong></td>
<td>300</td>
<td>460</td>
<td>873</td>
<td>1240</td>
<td>1100</td>
</tr>
<tr>
<td><strong>Intrinsic carrier density [cm⁻³] @ 25 °C</strong></td>
<td>$10^{10}$</td>
<td>$10^7$</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td><strong>Melting temperature [°C]</strong></td>
<td>1415</td>
<td>1238</td>
<td>Sublime</td>
<td>Sublime</td>
<td>Phase change</td>
</tr>
<tr>
<td><strong>Electron mobility @ 300 °K [cm²/V-sec]</strong></td>
<td>1400</td>
<td>8500</td>
<td>1000</td>
<td>600</td>
<td>2200</td>
</tr>
<tr>
<td><strong>Breakdown electric field [V/cm]</strong></td>
<td>2-3$x10^5$</td>
<td>$4 \times 10^5$</td>
<td>$2 \times 10^6$</td>
<td>$2 \times 10^6$</td>
<td>$1 \times 10^7$</td>
</tr>
</tbody>
</table>
On-State Resistance Comparison with Different Materials

- Specific drift region resistance of majority carrier device

\[ R_{\text{on}}^A \approx \frac{4q(BV_{\text{BD}})^2}{e^\text{m}_n(E_{\text{BD}})^3} \]

- Normalize to silicon - assume identical areas and breakdown voltages

\[ \frac{R_{\text{on}(x)}^A}{R_{\text{on}(\text{Si})}^A} = \text{resistance ratio} = \frac{e_{\text{Si}}^\text{m}_\text{Si}}{e_{x}^\text{m}_x} \left( \frac{E_{\text{BD, Si}}}{E_{\text{BD, x}}} \right)^3 \]

- Numerical comparison

<table>
<thead>
<tr>
<th>Material</th>
<th>Resistance Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>1</td>
</tr>
<tr>
<td>GaAs</td>
<td>6.4x10^{-2}</td>
</tr>
<tr>
<td>SiC</td>
<td>9.6x10^{-3}</td>
</tr>
<tr>
<td>Diamond</td>
<td>3.7x10^{-5}</td>
</tr>
</tbody>
</table>
Material Comparison: PN Junction Diode Parameters

- Approximate design formulas for doping density and drift region length of HV pn junctions
  - Based on step junction P⁺N⁻N⁺ structure
  - \( N_d = \text{drift region doping level} \approx \frac{e^{\frac{E_B D^2}{2qBV_{BD}}}}{qBV_{BD}} \)
  - \( W_d = \text{drift region length} \approx \frac{2qBV_{BD}}{E_B D} \)

- Numerical comparison - 1000 V breakdown rating

<table>
<thead>
<tr>
<th>Material</th>
<th>( N_d )</th>
<th>( W_d )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>1.3x10^{14} \text{ cm}^{-3}</td>
<td>67 \text{ ( \mu )m}</td>
</tr>
<tr>
<td>GaAs</td>
<td>5.7x10^{14}</td>
<td>50</td>
</tr>
<tr>
<td>SiC</td>
<td>1.1x10^{16}</td>
<td>10</td>
</tr>
<tr>
<td>Diamond</td>
<td>1.5x10^{17}</td>
<td>2</td>
</tr>
</tbody>
</table>
Material Comparison: Carrier Lifetime Requirements

- Drift region carrier lifetime required for 1000 V pn junction diode
- Approximate design formula based on step junction

\[ \tau \approx \frac{q W_d^2}{kT m_n} = \frac{4q [BV_{BD}]^2}{kT m_n [E_{BD}]^2} \]

- Numerical comparison

<table>
<thead>
<tr>
<th>Material</th>
<th>Lifetime</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>1.2 µsec</td>
</tr>
<tr>
<td>GaAs</td>
<td>0.11 µsec</td>
</tr>
<tr>
<td>SiC</td>
<td>40 nsec</td>
</tr>
<tr>
<td>Diamond</td>
<td>7 nsec</td>
</tr>
</tbody>
</table>

- Shorter carrier lifetimes mean faster switching minority carrier devices such as BJTs, pn junction diodes, IGBTs, etc.
Recent Advances/Benchmarks

• Gallium arsenide
  • 600V GaAs Schottky diodes announced by Motorola. 250V available from IXYS
  • 3” GaAs wafers available

• Silicon carbide
  • 3” wafers available from Cree Research - expensive
  • 600V -6A Schottky diodes available commercially - Infineon Technologies AG (Siemens spinoff)
  • Controlled switches also demonstrated
    • 1800V - 3A BJT with beta of 20
    • 3100V - 12A GTO

• Diamond
  • Polycrystalline diamond films of several micron thickness grown over large (square centimeters) areas
  • Simple device structures demonstrated in diamond films.
    • PN junctions
    • Schottky diodes
Projections

• GaAs
  • Devices such as Schottky diodes which are presently at or near commercial introduction will become available and used.
  • GaAs devices offer only incremental improvements in performance over Si devices compared to SiC or diamond.
  • Broad introduction of several types of GaAs-based power devices unlikely.

• SiC
  • Rapid advances in SiC device technology
  • Spurred by the great potential improvement in SiC devices compared to Si devices.
  • Commercially available SiC power devices within 5-10 years.

• Diamond
  • Research concentrated in improving materials technology.
    • Growth of single crystal material
    • Ancilliary materials issues - ohmic contacts, dopants, etc.
  • No commercially available diamond-based power devices in the foreseeable future (next 10-20 years).
Lecture Notes

Snubber Circuits

Outline

A. Overview of Snubber Circuits
B. Diode Snubbers
C. Turn-off Snubbers
D. Overvoltage Snubbers
E. Turn-on Snubbers
F. Thyristor Snubbers
Overview of Snubber Circuits for Hard-Switched Converters

Function: Protect semiconductor devices by:

- Limiting device voltages during turn-off transients
- Limiting device currents during turn-on transients
- Limiting the rate-of-rise (di/dt) of currents through the semiconductor device at device turn-on
- Limiting the rate-of-rise (dv/dt) of voltages across the semiconductor device at device turn-off
- Shaping the switching trajectory of the device as it turns on/off

Types of Snubber Circuits

1. Unpolarized series R-C snubbers
   - Used to protect diodes and thyristors

2. Polarized R-C snubbers
   - Used as turn-off snubbers to shape the turn-on switching trajectory of controlled switches.
   - Used as overvoltage snubbers to clamp voltages applied to controlled switches to safe values.
   - Limit dv/dt during device turn-off

3. Polarized L-R snubbers
   - Used as turn-on snubbers to shape the turn-off switching trajectory of controlled switches.
   - Limit di/dt during device turn-on
Need for Diode Snubber Circuit

- $L_s = \text{stray inductance}$
- $S_W$ closes at $t = 0$
- $R_s - C_s = \text{snubber circuit}$

- Diode breakdown if $V_d + L_s \frac{di}{dt} > BV_{BD}$
Equivalent Circuits for Diode Snubber

- Worst case assumption - diode snaps off instantaneously at end of diode recovery

- Simplified snubber - the capacitive snubber
  - $R_s = 0$
  - $v_{Cs} = -v_{Df}$

- Governing equation -
  \[ \frac{d^2 v_{Cs}}{dt^2} + \frac{v_{Cs}}{L_s C_s} = \frac{V_d}{L_s C_s} \]

- Boundary conditions -
  - $v_{Cs}(0^+) = 0$ and $i_{L_s}(0^+) = I_{rr}$
Performance of Capacitive Snubber

- \( v_{Cs}(t) = V_d - V_d \cos(\omega_0 t) + V_d \sqrt{\frac{C_{base}}{C_s}} \sin(\omega_0 t) \)

- \( \omega_0 = \frac{1}{\sqrt{L C_s}} \); \( C_{base} = L \)  

- \( V_{cs,\text{max}} = V_d 1 + \sqrt{1 + \frac{C_{base}}{C_s}} \)

\[
\frac{V_{Cs,\text{max}}}{V_d}
\]

\[
\frac{C_{base}}{C_s}
\]
Effect of Adding Snubber Resistance

Snubber Equivalent Circuit

- Governing equation: 
  \[
  L \frac{d^2i}{dt^2} + R_s \frac{di}{dt} + \frac{i}{C_s} = 0
  \]

- Boundary conditions:
  \[
  i(0^+) = I_{rr} \quad \text{and} \quad \frac{di(0^+)}{dt} = \frac{V_d - I_{rr}R_s}{L}
  \]

Diode voltage as a function of time

\[
\frac{V_{df}}{V_d}(t) = -1 - \frac{e^{-\Delta t}}{\sqrt{\Delta \cos(\Delta)}} \sin(\Delta a - \Delta + \Delta) \quad ; \quad R_s \leq 2 R_b
\]

\[
\Delta a = \Delta o \sqrt{1 - \left(\frac{\Delta}{\Delta o}\right)^2} \quad ; \quad \Delta = \frac{R_s}{2L} \quad ; \quad \Delta o = \frac{1}{\sqrt{L\Delta C_s}} \quad ; \quad x = \tan^{-1}\left[\frac{(2-x)\sqrt{\Delta}}{\sqrt{4 - x^2}}\right]
\]

\[
\Delta = \frac{C_s}{C_b} \quad ; \quad x = \frac{R_s}{R_b} \quad ; \quad R_b = \frac{V_d}{I_{rr}} \quad ; \quad C_b = \frac{L\left[I_{rr}\right]^2}{V_d^2} \quad ; \quad \Delta = \tan^{-1}\left(\frac{\Delta}{\Delta a}\right)
\]
Performance of R-C Snubber

- At $t = t_m$ $v_{Df}(t) = V_{\text{max}}$
- $t_m = \tan^{-1}\left(\frac{\omega_a}{\omega_a} + \frac{\omega - \omega_a}{\omega_a}\right) \geq 0$
- $\frac{V_{\text{max}}}{V_d} = 1 + \sqrt{1 + \left(\frac{\omega - \omega_a}{\omega_a}\right)^{-1} - x \exp(-\omega t_m)}$
- $\square = \frac{C_s}{C_{\text{base}}}$ and $x = \frac{R_s}{R_{\text{base}}}$
- $C_{\text{base}} = \frac{L_s}{V_d^2}$ and $R_{\text{base}} = \frac{V_d}{I_{\text{rr}}}$

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Snubbers - 7
Diode Snubber Design Nomogram

\[
\frac{W_{\text{tot}}}{L_s I_{rr}/2}
\]

\[
\frac{W_R}{L_s I_{rr}^2/2}
\]

\[
\frac{V_{\text{max}}}{V_d} \text{ for } R_s = R_{s,\text{opt}}
\]

\[
\frac{R_{s,\text{op}}}{R_{\text{base}}}
\]
Need for Snubbers with Controlled Switches

Step-down converter

Switch current and voltage waveforms

- $L_1, L_2, L_3 = \text{stray inductances}$

- $L = L_1 + L_2 + L_3$

Switching trajectory of switch

- Overvoltage at turn-off due to stray inductance
- Overcurrent at turn-on due to diode reverse recovery
Turn-off Snubber for Controlled Switches

Step-down converter with turn-off snubber

Equivalent circuit during switch turn-off.

- Simplifying assumptions
  1. No stray inductance.
  2. $i_{sw}(t) = I_0(1 - t/t_{ff})$
  3. $i_{sw}(t)$ unaffected by snubber circuit.
Turn-off Snubber Operation

- Capacitor voltage and current for $0 < t < t_{fi}$:
  \[ i_{Cs}(t) = \frac{l_o t}{t_{fi}} \quad \text{and} \quad v_{Cs}(t) = \frac{l_o t^2}{2C_s t_{fi}} \]

- For $C_s = C_{s1}$, $v_{Cs} = V_d$ at $t = t_{fi}$ yielding $C_{s1} = \frac{l_o t_{fi}}{2V_d}$

Circuit waveforms for varying values of $C_s$
Benefits of Snubber Resistance at Switch Turn-on

- $D_s$ shorts out $R_s$ during $S_w$ turn-off.
- During $S_w$ turn-on, $D_s$ reverse-biased and $C_s$ discharges thru $R_s$.

- Turn-on with $R_s = 0$
- Energy stored on $C_s$ dissipated in $S_w$.
- Extra energy dissipation in $S_w$ because of lengthened voltage fall time.

- Turn-on with $R_s > 0$
- Energy stored on $C_s$ dissipated in $R_s$ rather than in $S_w$.
- Voltage fall time kept quite short.
**Effect of Turn-off Snubber Capacitance**

Energy dissipation

- \( W_R \) = dissipation in resistor
- \( W_T \) = dissipation in switch \( S_W \)

\[
C_s = \frac{I_o t_{fi}}{2V_d}
\]

\( W_{\text{total}} = W_R + W_T \)

\( W_{\text{base}} = 0.5 \ V_d I_o t_{fi} \)

Switching trajectory
Turn-off Snubber Design Procedure

Selection of $C_S$

- Minimize energy dissipation ($W_T$) in BJT at turn-on
- Minimize $W_R + W_T$
- Keep switching locus within RBSOA
- Reasonable value is $C_S = C_{S1}$

Snubber recovery time (BJT in on-state)

- Capacitor voltage = $V_d \exp(-t/R_s C_s)$
- Time for $v_{C_S}$ to drop to 0.1$V_d$ is 2.3 $R_s C_s$
- BJT must remain on for a time of 2.3 $R_s C_s$

Selection of $R_s$

- Limit $i_{cap}^{(0^+)} = \frac{V_d}{R_s} < I_{rr}$
- Usually designer specifies $I_{rr} < 0.2 \ I_o$ so $\frac{V_d}{R_s} = 0.2 \ I_o$
**Overvoltage Snubber**

- Step-down converter with overvoltage snubber comprised of $D_{ov}$, $C_{ov}$, and $R_{ov}$.

- Overvoltage snubber limits overvoltage (due to stray inductance) across $S_w$ as it turns off.

- Switch $S_w$ waveforms without overvoltage snubber

- $t_{fi} =$ switch current fall time ; $kV_d =$ overvoltage on $S_w$
  
  - $kV_d = L \frac{di_{Li}}{dt} = L \frac{i_o}{t_{fi}}$

  - $L = \frac{kV_d t_{fi}}{i_o}$

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Operation of Overvoltage Snubber

- $D_{ov}, C_{ov}$ provide alternate path for inductor current as $S_w$ turns off.

- Switch current can fall to zero much faster than $L_s$ current.

- $D_f$ forced to be on (approximating a short ckt) by $I_o$ after $S_w$ is off.

- Equivalent circuit after turn-off of $S_w$.

\[ V_d \]

\[ i_{Ls} \]

\[ C_{ov} \]

\[ R_{ov} \]

\[ V_Cov \]

\[ i_{Ls}(t) = I_o \cos \left( \frac{t}{\sqrt{L_s C_{ov}}} \right) \]

Charge-up of $C_{ov}$ from $L_s$

\[ \Delta V_{sw, max} \]

Discharge of $C_{ov}$ thru $R_{ov}$ with time constant $R_{ov}C_{ov}$

\[ t_{fi} \ll \frac{\pi \sqrt{L_s C_{ov}}}{2} \]

- $D_{ov}$ on for $0 < t < \frac{\pi \sqrt{L_s C_{ov}}}{2}$

- $E_{sw}$ forced to be on (approximating a short ckt) by $I_o$ after $S_w$ is off.

\[ \frac{L_s (I_o)^2}{2} \]

\[ \frac{L_s (I_o)^2}{4} \]

\[ \frac{L_s (I_o) V_{sw, max}^2}{2} \]
Overvoltage Snubber Design

• \( C_{ov} = \frac{L_s I_o^2}{(\Delta v_{sw,max})^2} \)

• Limit \( \Delta v_{sw,max} \) to 0.1\( V_d \)

• Using \( L_s = \frac{kV_d t_{fi}}{I_o} \) in equation for \( C_{ov} \) yields

• \( C_{ov} = \frac{kV_d t_{fi} I_o^2}{I_o (0.1 V_d)^2} = \frac{100k t_{fi} I_o}{V_d} \)

• \( C_{ov} = 200k \ C_s1 \) where \( C_s1 = \frac{t_{fi} I_o}{2V_d} \) which is used in turn-off snubber

• Recovery time of \( C_{ov} (2.3R_{ov}C_{ov}) \) must be less than off-time duration, \( t_{off} \), of the switch Sw.

• \( R_{ov} \approx \frac{t_{off}}{2.3 \ C_{ov}} \)
**Turn-on Snubber**

**Step-down converter with turn-on snubber**

- Snubber reduces $V_{sw}$ at switch turn-on due drop across inductor $L_s$.
- Will limit rate-of-rise of switch current if $L_s$ is sufficiently large.

Switching trajectory with and without turn-on snubber.
Turn-on Snubber Operating Waveforms

Small values of snubber inductance ($L_s < L_{s1}$)

- $\frac{dV_{sw}}{dt}$ controlled by switch $S_w$ and drive circuit.

- $\Box V_{sw} = \frac{L_s I_o}{t_{ri}}$

Large values of snubber inductance ($L_s > L_{s1}$)

- $\frac{dV_{sw}}{dt}$ limited by circuit to $\frac{V_d}{L_s} < \frac{I_o}{t_{ri}}$

- $L_{s1} = \frac{V_d t_{ri}}{I_o}$

- $I_{rr}$ reduced when $L_s > L_{s1}$ because $I_{rr}$ proportional to $\sqrt{\frac{dV_{sw}}{dt}}$
Turn-on Snubber Recovery at Switch Turn-off

- Assume switch current fall time $t_{ri} = 0$.
- Inductor current must discharge thru $D_{Ls}$- $R_{Ls}$ series segment.

- Switch waveforms at turn-off with turn-on snubber in circuit.
- Overvoltage smaller if $t_{ri}$ smaller.
- Time of $2.3 \frac{L_s}{R_{Ls}}$ required for inductor current to decay to 0.1 $I_o$
- Off-time of switch must be $> 2.3 \frac{L_s}{R_{Ls}}$
Turn-on Snubber Design Trade-offs

**Selection of inductor**

- Larger $L_s$ decreases energy dissipation in switch at turn-on
  - $W_{sw} = W_B (1 + I_{rr}/I_o)^2 [1 - L / L_{s1}]$
  - $W_B = V_d I_o t_f / 2$ and $L_{s1} = V_d t_f / I_o$
  - $L_s > L_{s1}$ $W_{sw} = 0$

- Larger $L_s$ increases energy dissipation in $R_{LS}$
  - $W_R = W_B L_s / L_{s1}$

- $L_s > L_{s1}$ reduces magnitude of reverse recovery current $I_{rr}$

- Inductor must carry current $I_o$ when switch is on - makes inductor expensive and hence turn-on snubber seldom used

**Selection of resistor $R_{LS}$**

- Smaller values of $R_{LS}$ reduce switch overvoltage $I_o R_{LS}$ at turn-off

- Limiting overvoltage to $0.1V_d$ yields $R_{LS} = 0.1 V_d / I_o$

- Larger values of $R_{LS}$ shortens minimum switch off-time of $2.3 L_s / R_{LS}$
Thyristor Snubber Circuit

3-phase thyristor circuit with snubbers

- $v_{an}(t) = V_s \sin(\omega t)$, $v_{bn}(t) = V_s \sin(\omega t - 120^\circ)$,
- $v_{cn}(t) = V_s \sin(\omega t - 240^\circ)$

Phase-to-neutral waveforms

- $v_{LL}(t) = \sqrt{3} V_s \sin(\omega t - 60^\circ)$
- Maximum rms line-to-line voltage $V_{LL} = \frac{3}{2} V_s$
Equivalent Circuit for SCR Snubber Calculations

Assumptions

- Trigger angle $\phi = 90^\circ$ so that $v_{LL}(t) = \text{maximum} = \sqrt{2} \, V_{LL}$

- Reverse recovery time $t_{rr} << \text{period of ac waveform}$ so that $v_{LL}(t)$ equals a constant value of $v_{ba}(t_1) = \sqrt{2} \, V_{LL}$

- Worst case stray inductance $L_s$ gives rise to reactance equal to or less than 5% of line impedance.

- Line impedance $= \frac{V_s}{\sqrt{2}I_{a1}} = \frac{\sqrt{2}V_{LL}}{\sqrt{6}I_{a1}} = \frac{V_{LL}}{\sqrt[3]{3}I_{a1}}$

  where $I_{a1} = \text{rms value of fundamental component of the line current}$.  

- $L_s = 0.05 \frac{V_{LL}}{\sqrt[3]{3}I_{a1}}$

Equivalent circuit after T1 reverse recovery
Component Values for Thyristor Snubber

- Use same design as for diode snubber but adapt the formulas to the thyristor circuit notation

- Snubber capacitor $C_s = C_{\text{base}} = L \frac{l_{rr}}{\sqrt{d}}$

- From snubber equivalent circuit $2 L \frac{di_L}{dt} = \sqrt{2} V_{LL}$

- $I_{rr} = \frac{di_L}{dt} t_{rr} = \frac{\sqrt{2}V_{LL}}{2L} t_{rr} = \frac{\sqrt{2}V_{LL}}{0.05 V_{LL}} t_{rr} = 25 \frac{I_{a1} t_{rr}}{V_{LL}}$

- $V_d = \sqrt{2} V_{LL}$

- $C_s = C_{\text{base}} = \frac{0.05 V_{LL}}{\sqrt{3} I_{a1}} \frac{25 \frac{I_{a1} t_{rr}}{V_{LL}}}{\sqrt{2} V_{LL}} \frac{2}{V_{LL}} = \frac{8.7 I_{a1} t_{rr}}{V_{LL}}$

- Snubber resistance $R_s = 1.3 R_{\text{base}} = 1.3 \frac{V_d}{l_{rr}}$

- $R_s = 1.3 \frac{\sqrt{2}V_{LL}}{25 I_{a1} t_{rr}} = \frac{0.07 V_{LL}}{I_{a1} t_{rr}}$

- Energy dissipated per cycle in snubber resistance $= W_R$

- $W_R = \frac{L_{\text{base}} l_{rr}^2}{2} + \frac{C_s V_d^2}{2} = 18 \frac{I_{a1} V_{LL}}{2} (t_{rr})^2$
Drive Circuits

Outline

• Drive circuit design considerations
• DC-coupled drive circuits
• Isolated drive circuits
• Protection measures in drive circuits
• Component/circuit layout considerations
Functionality of Gate/Base Drive Circuits

- Turn power switch from off-state to on-state
  - Minimize turn-on time through active region where power dissipation is large
  - Provide adequate drive power to keep power switch in on-state

- Turn power switch from on-state to off-state
  - Minimize turn-off time through active region where power dissipation is large
  - Provide bias to insure that power switch remains off

- Control power switch to protect it when overvoltages or overcurrents are sensed

- Signal processing circuits which generate the logic control signals not considered part of the drive circuit
  - Drive circuit amplifies control signals to levels required to drive power switch
  - Drive circuit has significant power capabilities compared to logic level signal processing circuits

- Provide electrical isolation when needed between power switch and logic level signal processing/control circuits
Drive Circuit Design Considerations

- Drive circuit topologies
  - Output signal polarity - unipolar or bipolar
  - AC or DC coupled
  - Connected in shunt or series with power switch

- Output current magnitude
  - Large $I_{on}$ shortens turn-on time but lengthens turn-off delay time
  - Large $I_{off}$ shortens turn-off time but lengthens turn-on delay time

- Provisions for power switch protection
  - Overcurrents
  - Blanking times for bridge circuit drives

- Waveshaping to improve switch performance
  - Controlled $di_B/dt$ for BJT turn-off
  - Anti-saturation diodes for BJT drives
  - Speedup capacitors
  - Front-porch/backporch currents

- Component layout to minimize stray inductance and shielding from switching noise
Unipolar DC-coupled Drive Circuit - BJT Example

- Circuit operation
  - $V_{\text{control}} > V_{\text{reference}}$ - BJT at comparator output on which puts $Q_{\text{pnp}}$ and $Q_{\text{sw}}$ on
  - $V_{\text{control}} < V_{\text{reference}}$ - BJT at comparator output off which turns $Q_{\text{pnp}}$ off and thus $Q_{\text{sw}}$ off

- Design procedure
  - $R_2 = \frac{V_{\text{BE,off}}}{I_{\text{B,off}}}$; $I_{\text{B,off}}$ based on desired turn-off time.
  - $I_{\text{pnp}} = I_{\text{B,on}} + \frac{V_{\text{BE,on}}}{R_2}$; $I_{\text{B,on}}$ value based on BJT beta and value of $I_0$.
  - $V_{\text{BB}} = V_{\text{CE,on}}(Q_{\text{pnp}}) + R_1 I_{c,\text{pnp}} + V_{\text{BE,on}}(Q_{\text{sw}})$
  - $V_{\text{BB}} = 8$ to $10$ V; compromise between larger values which minimize effects of $V_{\text{BE}}$ variations and smaller values which minimize power dissipation in drive circuit.
Unipolar DC-coupled Drive Circuits - MOSFET examples

- \( V_{\text{control}} > V_{\text{reference}} \) comparator output high and \( Q_{\text{SW}} \) on
- \( V_{\text{control}} < V_{\text{reference}} \) comparator output low and \( Q_{\text{SW}} \) off

IC buffer amp with totem pole output DS0026 or UC1706/07
Bipolar DC-coupled Drive Circuit - BJT Example

- $V_{control} < V_{reference}$ - comparator output low, $T_B^-$ on and $Q_{sw}$ off.

- Large reverse base current flows to minimize turn-off time and base-emitter of $Q_{sw}$ reversed biased to insure off-state.

- $V_{control} > V_{reference}$ - comparator output high, $T_B^+$ on and $Q_{sw}$ on.

- Large forward base current to minimize turn-on time and to insure saturation of $Q_{sw}$ for low on-state losses.
Bipolar DC-coupled Drive Circuit- MOSFET Example

- Bipolar drive with substantial output current capability

IC buffer amp with totem pole output
DS0026 or UC1706/07

- Simple bipolar drive circuit with moderate (1 amp) output current capability
Need for Electrical Isolation of Drive Circuits

- Negative half cycle of $v_s(t)$ - positive dc rail near safety ground potential. $T_-$ emitter potential large and negative with respect to safety and logic ground.

- Positive half cycle of $v_s(t)$ - negative dc rail near safety ground potential. $T_+$ emitter substantially positive with respect to safety ground if $T_-$ is off.

- Variations in emitter potentials with respect to safety and logic ground means that electrical isolation of emitters from logic ground is needed.
Methods of Control Signal Isolation

- Transformer isolation
- Opto-coupler isolation
- Isolated dc power supplies for drive circuits
Opto-Coupler Isolated BJT Drive
Transformer-coupled BJT Drive

Oscillator

High frequency transformer

Fast signal diodes

Transformer primary voltage

Input to comparator

AC power input

Oscillator output

Vcontrol

Vcontrol

Transformer output

VBB+

VBB−
Opto-Coupler Isolated MOSFET Drives

Circuitry for isolated dc supplies not shown
Isolated Drives Without Auxiliary DC Supplies
- Proportional Flyback BJT Example

- Regenerative circuit operation

- $T_1$ on - current $i_p = \frac{V_{BB}}{R_p}$ and $Q_{sw}$ off

- $T_1$ turned off - stored energy in gapped transformer core induces positive base current $i_B$ in $Q_{sw}$ causing it to go active and collector current $i_C$ begins to flow

- Regenerative action of transformer connections supplies a base current $i_B = \frac{N_3i_C}{N_2}$ which keeps $Q_{sw}$ on even with $i_p = 0$

- $T_1$ turned on - positive current $i_p$ causes a base current $i_B = \frac{N_3i_C}{N_2} - \frac{N_1i_p}{N_2}$ in $Q_{sw}$
  - Initially $i_p$ quite large ($i_p(0^+) = [i_B(0^+)]$) so $Q_{sw}$ turned off

- Circuit design must insure turn-off $i_B$ has adequate negative magnitude and duration

- Best suited for high frequency operation - lower volt-second requirements on transformer.

- Also best suited for limited variations in duty cycle
Isolated Drives Without Auxiliary DC Supplies
- MOSFET Example

Most suitable for applications where duty cycle D is 50% or less. Positive-going secondary voltage decreases as D increases.
Isolated Drive Without Auxiliary DC Supplies - MOSFET Example

Zener diode voltage $V_Z$ must be less than negative pulse out of transformer secondary or pulse will not reach MOSFET gate to turn it off.
Isolated Drive Without Auxiliary DC Supplies
- MOSFET Example

The diagram illustrates a circuit with an oscillator, buffers, transistors, and capacitors. Key components include:

- **4011** and **4047** oscillators
- **7555** timer
- **4011** buffer
- **4047** buffer
- Resistors (R1, R2)
- Capacitors (C1, C2)
- Diodes (D1, D2)
- MOSFET (Q)

Key points:

- **vcontrol**
- **vQ**
- **vQ**
- **vtrans**
- **v1s**
- **v2s**

Decay of voltage on C2 via R2.

C1 charges up to a positive voltage at power-up and remains there. D1 prevents discharge.
Emitter-Open Switching of BJTs

- Circuit operation
  - Turn on power BJT by turning on MOSFET $T_E$.
  - Turn off power BJT by turning off MOSFET $T_E$.
    - Collector current flows out base as negative base current.
  - Greater $i_B(\text{off})$ compared to standard drive circuits $i_C = b_i B(\text{off})$ removes stored charge much faster
    - Turn off times reduced (up to ten times).

- On-state losses of series combination of MOSFET and BJT minimized.
  - Low voltage MOSFET which has low losses can be used. Maximum off-state MOSFET voltage limited by Zener diode.
  - BJT base emitter junction reverse biased when $T_E$ off so breakdown rating of BJT given by $BV_{CEO}$ instead of $BV_{CBO}$. With lower $BV_{CEO}$ rating, BJT losses in on-state reduced.

- Circuit also useful for GTOs and FCTs.
Thyristor Gate Drive Circuit

Line Voltage

Delay Angle Block

Input Control Signal

Control Logic Ground

Gate pulse isolation transformers

Pulse Amplifier

Gate pulse isolation transformers

DC power supply for gate trigger circuit

Zero crossing detection

Delay angle block is commercially available integrated circuit - TCA780 circuit family
Thyristor Gate Drive Circuit (cont.)

Thyristor gate drive waveforms

Gate pulse amplifier
GTO Gate Drive Circuit

- Turn on $T_G1$ and $T_G2$ to get large front-porch current
- Turn off $T_G1$ after some specified time to reduce total gate current to back-porch value.
Overcurrent Protection With Drive Circuits

- Point C one diode drop above $V_{CE(sat)}$ when BJT is on. Overcurrent will increase $V_{CE}$ and thus potential at C.

- If C rises above a threshold value and control signal is biasing BJT on, overcurrent protection block will turn off BJT. Conservate design would keep BJT off until a manual reset had been done.
Limiting Overcurrents by Limiting On-state Base Current

- Stepdown converter with short circuit at $t = t_{sc}$

- Overcurrent limited to $I_{C(on)max} < I_{C,sc}$ by keeping $I_{B,max} < I_{C,sc}/b$

- $I_{C,sc}$ = maximum allowable instantaneous collector current

- Same approach can be used with MOSFETs and IGBTs. $V_{GS}$ must be restricted to keep drain current to safe values.
Blanking Times in Bridge Circuit Drives

- Turn off T+ before turning on T- in order to avoid cross-conduction (shorting out of Vd)

Diagram showing the control signals and timing for blanking times in bridge circuit drives.
Drive Circuit Waveshaping for Improved Operation

- Anti-saturation diode $D_{as}$ keeps $Q_{sw}$ active.
- $V_{AE} = V_{BE(on)} + V_{D1} = V_{CE(on)} + V_{das}$
- $V_{CE(on)} = V_{BE(on)} > V_{CE(sat)}$ because $V_{D1} = V_{das}$
- $D_{s}$ provides path for negative base current at $Q_{sw}$ turn-off.
- Storage delay time at turn-off reduced but on-state losses increase slightly.

Speed-up capacitors

- Transient overdrive provided via $C_{on}$ for faster turn-on of switch
- Same concept can be applied to MOSFET and IGBT drive circuits
Controlled rate of change of turn-off base current

- Excessively long collector current tailing time at BJT turn-off if $\frac{di_B(\text{off})}{dt}$ is too large.
- Inductor $L_{\text{off}}$ restricts $\frac{di_B(\text{off})}{dt}$ to $-\frac{V_{BB}}{L_{\text{off}}}$

Front porch, back porch gate/base currents at turn-on

- Faster turn-on without putting device deeply into on-state where turn-off delay time will be substantially increased.
- Applicable to BJTs, MOSFETs, IGBTs, and GTOs.
Circuit/Component Layout Considerations

Prime consideration is minimizing stray inductance

- Stray inductance in series with high-voltage side of power device $Q_{sw}$ causes overvoltage at turn-off.
- Stray inductance in series with low-voltage side power device $Q_{sw}$ can cause oscillations at turn-on and turn-off.
- One cm of unshielded lead has about 5 nH of series inductance.
- Keep unshielded lead lengths to an absolute minimum.

Use shielded conductors to connect drive circuit to power switch if there must be any appreciable separation (few cm or more) between them

Some power devices provided with four leads, two input leads and two power leads, to minimize stray inductance in input circuit.

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Heat Sinks and Component Temperature Control
Need for Component Temperature Control

- All components, capacitors, inductors and transformers, and semiconductor devices and circuits have maximum operating temperatures specified by manufacturer.
- Component reliability decreases with increasing temperature. Semiconductor failure rate doubles for every 10 - 15 °C increase in temperature above 50 °C (approx. rule-of-thumb).

- High component operating temperatures have undesirable effects on components.

<table>
<thead>
<tr>
<th>Capacitors</th>
<th>Magnetic Components</th>
<th>Semiconductors</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrolyte evaporation rate increases significantly with temperature increases and thus shortens lifetime.</td>
<td>• Losses (at constant power input) increase above 100 °C</td>
<td>• Unequal power sharing in paralleled or seriesed devices.</td>
</tr>
<tr>
<td></td>
<td>• Winding insulation (lacquer or varnish) degrades above 100 °C</td>
<td>• Reduction in breakdown voltage in some devices.</td>
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<tr>
<td></td>
<td></td>
<td>• Increase in leakage currents.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Increase in switching times.</td>
</tr>
</tbody>
</table>
Temperature Control Methods

• Control voltages across and current through components via good design practices.
  • Snubbers may be required for semiconductor devices.
  • Free-wheeling diodes may be needed with magnetic components.

• Use components designed by manufacturers to maximize heat transfer via convection and radiation from component to ambient.
  • Short heat flow paths from interior to component surface and large component surface area.

• Component user has responsibility to properly mount temperature-critical components on heat sinks.
  • Apply recommended torque on mounting bolts and nuts and use thermal grease between component and heat sink.
  • Properly design system layout and enclosure for adequate air flow so that heat sinks can operate properly to dissipate heat to the ambient.
Heat Conduction Thermal Resistance

- Generic geometry of heat flow via conduction

- Heat flow $P_{\text{cond}} [\text{W/m}^2] = \frac{\square A (T_2 - T_1)}{d} = \frac{(T_2 - T_1)}{R_{\text{cond}}}$

- Thermal resistance $R_{\text{cond}} = \frac{d}{[\square A]}$
  - Cross-sectional area $A = hb$
  - $\square = \text{Thermal conductivity has units of W-m}^{-1}{-^\circ}\text{C}^{-1}$ ($\square_{\text{Al}} = 220 \text{ W-m}^{-1}{-^\circ}\text{C}^{-1}$).
  - Units of thermal resistance are ${^\circ}\text{C/W}$
Thermal Equivalent Circuits

- Heat flow through a structure composed of layers of different materials.
- Thermal equivalent circuit simplifies calculation of temperatures in various parts of structure.

\[ T_i = P_d (R_{jc} + R_{cs} + R_{sa}) + T_a \]

- If there parallel heat flow paths, then thermal resistances of the parallel paths combine as do electrical resistors in parallel.
Transient Thermal Impedance

- Heat capacity per unit volume $C_v = \frac{dQ}{dT}$ [Joules /°C] prevents short duration high power dissipation surges from raising component temperature beyond operating limits.

- Transient thermal equivalent circuit. $C_s = C_v V$ where $V$ is the volume of the component.

- Transient thermal impedance $Z_q(t) = \frac{T_j(t) - T_a}{P(t)}$

  - $\tau = \pi R_q C_s / 4 = \text{thermal time constant}$
  - $T_j(t = \tau) = 0.833 P_o R_q$
Application of Transient Thermal Impedance

- Symbolic response for a rectangular power dissipation pulse $P(t) = P_o \{u(t) - u(t - t_1)\}$.

- $T_j(t) = P_o \{ Z(t) - Z(t - t_1) \}$

- Symbolic solution for half sine power dissipation pulse.
  - $P(t) = P_o \{u(t - T/8) - u(t - 3T/8)\}$ ; area under two curves identical.
  - $T_j(t) = P_o \{ Z(t - T/8) - Z(t - 3T/8) \}$
Z for Multilayer Structures

- Multilayer geometry

- Transient thermal equivalent circuit

- Transient thermal impedance (asymptotic) of multilayer structure assuming widely separated thermal time constants.

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Heat Sinks

- Aluminum heat sinks of various shapes and sizes widely available for cooling components.
  - Often anodized with black oxide coating to reduce thermal resistance by up to 25%.
  - Sinks cooled by natural convection have thermal time constants of 4 - 15 minutes.
  - Forced-air cooled sinks have substantially smaller thermal time constants, typically less than one minute.

- Choice of heat sink depends on required thermal resistance, $R_{sa}$, which is determined by several factors.
  - Maximum power, $P_{diss}$, dissipated in the component mounted on the heat sink.
  - Component's maximum internal temperature, $T_{j,max}$
  - Component's junction-to-case thermal resistance, $R_{jc}$.
  - Maximum ambient temperature, $T_{a,max}$.

$$R_{sa} = \left( T_{j,max} - T_{a,max} \right) P_{diss} - R_{jc}$$

- $P_{diss}$ and $T_{a,max}$ determined by particular application.
- $T_{j,max}$ and $R_{jc}$ set by component manufacturer.
Radiative Thermal Resistance

• Stefan-Boltzmann law describes radiative heat transfer.
  • \( P_{\text{rad}} = 5.7 \times 10^{-8} EA \left[ \left( \frac{T_s}{100} \right)^4 - \left( \frac{T_a}{100} \right)^4 \right] \); \([P_{\text{rad}}]\) = [watts]
  • \( E \) = emissivity; black anodized aluminum \( E = 0.9 \); polished aluminum \( E = 0.05 \)
  • \( A \) = surface area [m²] through which heat radiation emerges.
  • \( T_s \) = surface temperature [°K] of component. \( T_a \) = ambient temperature [°K].

\[ \frac{(T_s - T_a)}{P_{\text{rad}}} = R_{\text{rad}} = \frac{1}{[T_s - T_a][5.7EA \left( \frac{T_s}{100} \right)^4 - \left( \frac{T_a}{100} \right)^4]} \]

• Example - black anodized cube of aluminum 10 cm on a side. \( T_s = 120 \) °C and \( T_a = 20 \) °C
  • \( R_{\text{rad}} = \frac{1}{[393 - 293][(5.7)(0.9)(6 \times 10^{-2})\{(393/100)^4 - (293/100)^4\}]} \)
  • \( R_{\text{rad}} = 2.2 \) °C/W
Convective Thermal Resistance

- $P_{\text{conv}} = \text{convective heat loss to surrounding air from a vertical surface at sea level having a height } d_{\text{vert}} \text{ [in meters] less than one meter.}$
  - $P_{\text{conv}} = 1.34 \ A \ [T_s - T_a]^{1.25} \ d_{\text{vert}}^{-0.25}$
  - $A = \text{total surface area in [m}^2\text{]}$
  - $T_s = \text{surface temperature [°K] of component. } T_a = \text{ambient temperature [°K].}$

- \[
\frac{[T_s - T_a]}{P_{\text{conv}}} = R_{\text{conv}} = [T_s - T_a] \ [d_{\text{vert}}]^{0.25} [1.34 \ A \ (T_s - T_a)^{1.25}]^{-1}
\]
  - $R_{\text{conv}} = [d_{\text{vert}}]^{0.25} \ {1.34 \ A \ [T_s - T_a]^{0.25}}^{-1}$

- Example - black anodized cube of aluminum 10 cm on a side. $T_s = 120$ °C and $T_a = 20$ °C.
  - $R_{\text{conv}} = [10^{-1}]0.25([1.34] \ [6 \times 10^{-2}] \ [120 - 20]^{0.25})^{-1}$
  - $R_{\text{conv}} = 2.2$ °C/W
Combined Effects of Convection and Radiation

- Heat loss via convection and radiation occur in parallel.

- Steady-state thermal equivalent circuit

- \[ R_{\text{sink}} = \frac{R_{\text{rad}} R_{\text{conv}}}{R_{\text{rad}} + R_{\text{conv}}} \]

- Example - black anodized aluminum cube 10 cm per side

- \[ R_{\text{rad}} = 2.2 \, ^\circ\text{C/W} \] and \[ R_{\text{conv}} = 2.2 \, ^\circ\text{C/W} \]

- \[ R_{\text{sink}} = \frac{(2.2)(2.2)}{(2.2 + 2.2)} = 1.1 \, ^\circ\text{C/W} \]
Design of Magnetic Components

Outline

A. Inductor/Transformer Design Relationships
B. Magnetic Cores and Materials
C. Power Dissipation in Copper Windings
D. Thermal Considerations
E. Analysis of Specific Inductor Design
F. Inductor Design Procedures
G. Analysis of Specific Transformer Design
H. Eddy Currents
J. Transformer Leakage Inductance
K. Transformer Design Procedures
Magnetic Component Design Responsibility of Circuit Designer

- Ratings for inductors and transformers in power electronic circuits vary too much for commercial vendors to stock full range of standard parts.

- Instead only magnetic cores are available in a wide range of sizes, geometries, and materials as standard parts.

- Circuit designer must design the inductor/transformer for the particular application.

- Design consists of:

  1. Selecting appropriate core material, geometry, and size

  2. Selecting appropriate copper winding parameters: wire type, size, and number of turns.

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Review of Inductor Fundamentals

- **Assumptions**
  - No core losses or copper winding losses
  - Linearized B-H curve for core with $m >> m_o$
  - $i_m >> g$ and $A >> g^2$
  - Magnetic circuit approximations (flux uniform over core cross-section, no fringing flux)

- **Starting equations**
  - $H_m i_m + H_g g = N I$ (Ampere’s Law)
  - $B_m A = B_g A = \square$ (Continuity of flux assuming no leakage flux)
  - $m H_m = B_m$ (linearized B-H curve);
    $m_o H_g = B_g$

- **Results**
  - $B_S > B_m = B_g = \frac{N I}{i_m/m + g/m_o} = \square/A$
  - $LI = N\square$; $L = \frac{A N^2}{i_m/m + g/m_o}$

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Review of Transformer Fundamentals

• Assumptions same as for inductor

• Starting equations
  • \( H_1 L_m = N_1 I_1 \); \( H_2 L_m = N_2 I_2 \)
    (Ampere's Law)
  • \( H_m L_m = (H_1 - H_2) L_m = N_1 I_1 - N_2 I_2 \)
  • \( \mu_m H_m = B_m \) (linearized B-H curve)
  • \( v_1 = N_1 \frac{d\Phi_1}{dt} \); \( v_2 = N_2 \frac{d\Phi_2}{dt} \)
    (Faraday's Law)
  • Net flux \( \Phi = \Phi_1 - \Phi_2 = \mu_m H_m A \)
    \( \frac{\mu_m A (N_1 I_1 - N_2 I_2)}{L_m} \)

• Results assuming \( \mu_m \Phi = 0 \), i.e. ideal core or ideal transformer approximation.
  • \( \frac{\Phi}{\mu_m} = 0 \) and thus \( N_1 I_1 = N_2 I_2 \)
  • \( \frac{d(\Phi_1 - \Phi_2)}{dt} = 0 = \frac{v_1}{N_1} - \frac{v_2}{N_2} \); \( \frac{v_1}{N_1} = \frac{v_2}{N_2} \)
Current/Flux Density Versus Core Size

- Larger electrical ratings require larger current $I$ and larger flux density $B$.

- Core losses (hysteresis, eddy currents) increase as $B^2$ (or greater)

- Winding (ohmic) losses increase as $I^2$ and are accentuated at high frequencies (skin effect, proximity effect)

- To control component temperature, surface area of component and thus size of component must be increased to reject increased heat to ambient.

- At constant winding current density $J$ and core flux density $B$, heat generation increases with volume $V$ but surface area only increases as $V^{2/3}$.

- Maximum $J$ and $B$ must be reduced as electrical ratings increase.

- Flux density $B$ must be $< B_s$
  - Higher electrical ratings $\square$ larger total flux
  $\square$ larger component size

- Flux leakage, nonuniform flux distribution complicate design
Magnetic Component Design Problem

- Challenge - conversion of component operating specs in converter circuit into component design parameters.

- Goal - simple, easy-to-use procedure that produces component design specs that result in an acceptable design having a minimum size, weight, and cost.

- Inductor electrical (e.g. converter circuit) specifications.
  - Inductance value $L$
  - Inductor currents rated peak current $I_{\text{pr}}$, rated rms current $I_{\text{rms}}$, and rated dc current (if any) $I_{\text{dc}}$
  - Operating frequency $f$
  - Allowable power dissipation in inductor or equivalently maximum surface temperature of the inductor $T_s$ and maximum ambient temperature $T_a$.

- Transformer electrical (converter circuit) specifications.
  - Rated rms primary voltage $V_{\text{pri}}$
  - Rated rms primary current $I_{\text{pri}}$
  - Turns ratio $N_{\text{pri}}/N_{\text{sec}}$
  - Operating frequency $f$
  - Allowable power dissipation in transformer or equivalently maximum temperatures $T_s$ and $T_a$.

- Design procedure outputs.
  - Core geometry and material.
  - Core size $(A_{\text{core}}, A_w)$
  - Number of turns in windings.
  - Conductor type and area $A_{\text{cu}}$.
  - Air gap size (if needed).

- Three impediments to a simple design procedure.
  1. Dependence of $J_{\text{rms}}$ and $B$ on core size.
  2. How to chose a core from a wide range of materials and geometries.
  3. How to design low loss windings at high operating frequencies.

- Detailed consideration of core losses, winding losses, high frequency effects (skin and proximity effects), heat transfer mechanisms required for good design procedures.
Core Shapes and Sizes

- Magnetic cores available in a wide variety of sizes and shapes.
  - Ferrite cores available as U, E, and I shapes as well as pot cores and toroids.
  - Laminated (conducting) materials available in E, U, and I shapes as well as tape wound toroids and C-shapes.
  - Open geometries such as E-core make for easier fabrication but more stray flux and hence potentially more severe EMI problems.
  - Closed geometries such as pot cores make for more difficult fabrication but much less stray flux and hence EMI problems.

- Bobbin or coil former provided with most cores.

- Dimensions of core are optimized by the manufacturer so that for a given rating (i.e. stored magnetic energy for an inductor or V-I rating for a transformer), the volume or weight of the core plus winding is minimized or the total cost is minimized.
  - Larger ratings require larger cores and windings.
  - Optimization requires experience and computerized optimization algorithm.
  - Vendors usually are in much better position to do the optimization than the core user.
Double-E Core Example

Core

Bobbin

Assembled core and winding

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Relative Size</th>
<th>Absolute Size for ( a = 1 \text{ cm} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core area ( A_{\text{core}} )</td>
<td>1.5 ( a^2 )</td>
<td>1.5 ( \text{cm}^2 )</td>
</tr>
<tr>
<td>Winding area ( A_{\text{w}} )</td>
<td>1.4 ( a^2 )</td>
<td>1.4 ( \text{cm}^2 )</td>
</tr>
<tr>
<td>Area product ( A_{\text{w}} A_{\text{c}} )</td>
<td>2.1 ( a^4 )</td>
<td>2.1 ( \text{cm}^4 )</td>
</tr>
<tr>
<td>Core volume ( V_{\text{core}} )</td>
<td>13.5 ( a^3 )</td>
<td>13.5 ( \text{cm}^3 )</td>
</tr>
<tr>
<td>Winding volume ( V_{\text{w}} )</td>
<td>12.3 ( a^3 )</td>
<td>12.3 ( \text{cm}^3 )</td>
</tr>
<tr>
<td>Total surface area of assembled core and winding</td>
<td>59.6 ( a^2 )</td>
<td>59.6 ( \text{cm}^2 )</td>
</tr>
</tbody>
</table>
Types of Core Materials

- Iron-based alloys
  - Various compositions
    - Fe-Si (few percent Si)
    - Fe-Cr-Mn
    - METGLASS (Fe-B, Fe-B-Si, plus many other compositions)
  - Important properties
    - Resistivity $\rho = (10 - 100) \, \Omega \cdot \text{Cu}
    - $B_S = 1 - 1.8 \, \text{T (T = tesla = 10}^4 \, \text{oe)}$
  - METGLASS materials available only as tapes of various widths and thickness.
  - Other iron alloys available as laminations of various shapes.
  - Powdered iron can be sintered into various core shapes. Powdered iron cores have larger effective resistivities.

- Ferrite cores
  - Various compositions - iron oxides, Fe-Ni-Mn oxides
  - Important properties
    - Resistivity very large (insulator) - no ohmic losses and hence skin effect problems at high frequencies.
    - $B_S = 0.3 \, \text{T (T = tesla = 10}^4 \, \text{oe)}$
Hysteresis Loss in Magnetic Materials

- Area encompassed by hysteresis loop equals work done on material during one cycle of applied ac magnetic field. Area times frequency equals power dissipated per unit volume.

- Typical waveforms of flux density, $B(t)$ versus time, in an inductor.

- Only $B_{ac}$ contributes to hysteresis loss.
Quantitative Description of Core Losses

- Eddy current loss plus hysteresis loss = core loss.

- Empirical equation - $P_{m,sp} = k f^a [B_{ac}]^d$
  
  $f =$ frequency of applied field. $B_{ac} =$ base-to-peak value of applied ac field. $k$, $a$, and $d$ are constants which vary from material to material

- $P_{m,sp} = 1.5 \times 10^{-6} f^{1.3} [B_{ac}]^{2.5}$
  mW/cm$^3$ for 3F3 ferrite. (f in kHz and B in mT)

- $P_{m,sp} = 3.2 \times 10^{-6} f^{1.8} [B_{ac}]^{2}$
  mW/cm$^3$ METGLAS 2705M (f in kHz and B in mT)

- Example: 3F3 ferrite with $f = 100$ kHz and $B_{ac} = 100$ mT, $P_{m,sp} = 60$ mW/cm$^3$

3F3 core losses in graphical form.
Core Material Performance Factor

- Volt-amp (V-A) rating of transformers proportional to $f B_{ac}$

- Core materials have different allowable values of $B_{ac}$ at a specific frequency. $B_{ac}$ limited by allowable $P_{m,sp}$.

- Most desirable material is one with largest $B_{ac}$.

- Choosing best material aided by defining an empirical performance factor $PF = f B_{ac}$. Plots of PF versus frequency for a specified value of $P_{m,sp}$ permit rapid selection of best material for an application.

- Plot of PF versus frequency at $P_{m,sp} = 100$ mW/cm$^3$ for several different ferrites shown below.
Eddy Current Losses in Magnetic Cores

- AC magnetic fields generate eddy currents in conducting magnetic materials.
- Eddy currents dissipate power.
- Shield interior of material from magnetic field.

\[ \frac{B_i(r)}{B_o} = \exp\left(\frac{r - a}{\delta}\right) \]

\[ \delta = \text{skin depth} = \sqrt{\frac{2}{\sigma \mu_0 f}} \]

- \( \delta = 2\pi f, f = \text{frequency} \)
- \( \delta = \text{magnetic permeability} ; \quad \mu_0 \text{ for magnetic materials.} \)
- \( \sigma = \text{conductivity of material.} \)

Numerical example

- \( \sigma = 0.05 \, \text{Cu} ; \quad \mu = 10^3 \, \mu_0 \)
- \( f = 100 \, \text{Hz} \)
- \( \delta = 1 \, \text{mm} \)
Laminated Cores

- Cores made from conductive magnetic materials must be made of many thin laminations. Lamination thickness < skin depth.

- Stacking factor $k_{stack} = \frac{t}{t + 0.05t}$
Eddy Current Losses in Laminated Cores

- Flux $\Phi(t)$ intercepted by current loop of area $2xw$ given by $\Phi(t) = 2xwB(t)$

- Voltage in current loop $v(t) = 2xw \frac{dB(t)}{dt} = 2wxB\cos(\omega t)$

- Current loop resistance $r = \frac{2wL_{core}}{dx}, \ w \gg d$

- Instantaneous power dissipated in thin loop
  $$p(t) = \frac{[v(t)]^2}{r}$$

- Average power $P_{ec}$ dissipated in lamination
  given by
  $$P_{ec} = \frac{w L d^3 4 B^2}{24 L_{core}}$$

- $P_{ec,sp} = \frac{P_{ec}}{V} = \frac{w L d^3 4 B^2}{24 L_{core} \ dwL} = \frac{d^2 4 B^2}{24 L_{core}}$
Power Dissipation in Windings

- Average power per unit volume of copper dissipated in copper winding = $P_{cu,sp} = \rho_{cu} (J_{rms})^2$ where $J_{rms} = I_{rms}/A_{cu}$ and $\rho_{cu} =$ copper resistivity.

- Average power dissipated per unit volume of winding = $P_{w,sp} = k_{cu} \rho_{cu} (J_{rms})^2$ ; $V_{cu} = k_{cu} V_{w}$ where $V_{cu} =$ total volume of copper in the winding and $V_{w} =$ total volume of the winding.

- Copper fill factor $k_{cu} = \frac{N A_{cu}}{A_w} < 1$

- $N =$ number of turns; $A_{cu} =$ cross-sectional area of copper conductor from which winding is made; $A_w = b_w l_w =$ area of winding window.

- $k_{cu} = 0.3$ for Leitz wire; $k_{cu} = 0.6$ for round conductors; $k_{cu} \approx 0.7-0.8$ for rectangular conductors.

- $k_{cu} < 1$ because:
  - Insulation on wire to avoid shorting out adjacent turns in winding.
  - Geometric restrictions. (e.g. tight-packed circles cannot cover 100% of a square area.)

Double-E core example

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Eddy Currents Increase Winding Losses

- AC currents in conductors generate ac magnetic fields which in turn generate eddy currents that cause a nonuniform current density in the conductor. Effective resistance of conductor increased over dc value.
  - \( P_{w,sp} > k_{cu} \Delta_{cu} (J_{rms})^2 \) if conductor dimensions greater than a skin depth.
  - \( \frac{J(r)}{J_o} = \exp(\{r - a\}/ \|) \)
  - \( \| = \text{skin depth} = \sqrt{2 \mu_0 m_s} \)
    - \( \| = 2\pi f, f = \text{frequency of ac current} \)
    - \( \| = \text{magnetic permeability of conductor; } \| = \|_o \) for nonmagnetic conductors.
    - \( s = \text{conductivity of conductor material.} \)

- Numerical example using copper at 100 °C

<table>
<thead>
<tr>
<th>Frequency</th>
<th>50 Hz</th>
<th>5 kHz</th>
<th>20 kHz</th>
<th>500 kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Skin Depth</td>
<td>10.6 mm</td>
<td>1.06 mm</td>
<td>0.53 mm</td>
<td>0.106 mm</td>
</tr>
</tbody>
</table>

- Minimize eddy currents using Leitz wire bundle. Each conductor in bundle has a diameter less than a skin depth.
- Twisting of paralleled wires causes effects of intercepted flux to be canceled out between adjacent twists of the conductors. Hence little if any eddy currents.
Proximity Effect Further Increases Winding Losses

- Proximity effect - losses due to eddy current generated by the magnetic field experienced by a particular conductor section but generated by the current flowing in the rest of the winding.

- Design methods for minimizing proximity effect losses discussed later.
Minimum Winding Loss

- $P_w = P_{dc} + P_{ec}$; $P_{ec}$ = eddy current loss.
- $P_w = \{ R_{dc} + R_{ec}\} [I_{rms}]^2 = R_{ac} [I_{rms}]^2$
- $R_{ac} = FR_{dc} R_{dc} = [1 + R_{ec}/R_{dc}] R_{dc}$
- Minimum winding loss at optimum conductor size.
  - $P_w = 1.5 P_{dc}$
  - $P_{ec} = 0.5 P_{dc}$
- High frequencies require small conductor sizes minimize loss.
- $P_{dc}$ kept small by putting may small-size conductors in parallel using Litz wire or thin but wide foil conductors.

Optimum conductor size

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Thermal Considerations in Magnetic Components

- Losses (winding and core) raise core temperature. Common design practice to limit maximum interior temperature to 100-125 °C.

- Core losses (at constant flux density) increase with temperature increases above 100 °C.

- Saturation flux density $B_s$ decreases with temp. Increases.

- Nearby components such as power semiconductor devices, integrated circuits, capacitors have similar limits.

- Temperature limitations in copper windings:
  - Copper resistivity increases with temperature increases. Thus losses, at constant current density increase with temperature.
  - Reliability of insulating materials degrade with temperature increases.

- Surface temperature of component nearly equal to interior temperature. Minimal temperature gradient between interior and exterior surface.
  - Power dissipated uniformly in component volume.
  - Large cross-sectional area and short path lengths to surface of components.
  - Core and winding materials have large thermal conductivity.

- Thermal resistance (surface to ambient) of magnetic component determines its temperature.

$$ P_{sp} = \frac{T_s - T_a}{R_{sa}(V_w + V_c)} ; \quad R_{sa} = \frac{h}{A_s} $$

- $h$ = convective heat transfer coefficient = 10 °C-m²/W
- $A_s$ = surface area of inductor (core + winding).
  Estimate using core dimensions and simple geometric considerations.

- Uncertain accuracy in $h$ and other heat transfer parameters do not justify more accurate thermal modeling of inductor.
Scaling of Core Flux Density and Winding Current Density

- Power per unit volume, $P_{sp}$, dissipated in magnetic component is $P_{sp} = k_1/a$ ; $k_1$ = constant and $a$ = core scaling dimension.

- $P_{w,sp} V_w + P_{m,sp} V_m = \frac{T_s - T_a}{R_{sa}}$:
  
  $T_a$ = ambient temperature and $R_{sa}$ = surface-to-ambient thermal resistance of component.

- For optimal design $P_{w,sp} = P_{c,sp} = P_{sp}$:
  
  Hence $P_{sp} = \frac{T_s - T_a}{R_{sa}(V_w + V_c)}$

- $R_{sa}$ proportional to $a^2$ and $(V_w + V_c)$ proportional to $a^3$

- $J_{rms} = \sqrt{\frac{P_{sp}}{k_{cu} r_{cu}}} = k_2 \frac{1}{\sqrt{k_{cu} a}}$ ; $k_2$ = constant

- $P_{m,sp} = P_{sp} = k f_b [B_{ac}]^d$ ; Hence
  
  $B_{ac} = \sqrt{\frac{P_{sp}}{k f_b}} = \frac{k_3}{\sqrt{f_b} a}$ where $k_3$ = constant

- Plots of $J_{rms}$, $B_{ac}$, and $P_{sp}$ versus core size (scale factor $a$) for a specific core material, geometry, frequency, and $T_s - T_a$ value very useful for picking appropriate core size and winding conductor size.
Example of Power Density and Current Density Scaling

Assumptions

1. Double-E core made from 3F3 ferrite
2. $T_s = 100$ °C and $T_a = 40$ °C.
3. Winding made with Leitz wire - $k_{cu} = 0.3$
Analysis of a Specific Inductor Design

- Inductor specifications
  - Maximum current = 4 ams rms at 100 kHz
  - Double-E core with a = 1 cm using 3F3 ferrite.
  - Distributed air-gap with four gaps, two in series in each leg; total gap length \( g \) = 3 mm.
  - Winding - 66 turns of Leitz wire with \( A_{cu} = 0.64 \text{ mm}^2 \)
  - Inductor surface black with emissivity = 0.9
  - \( T_{a,max} = 40^\circ \text{C} \)

- Find; inductance \( L \), \( T_{s,max} \); effect of a 25% overcurrent on \( T_s \)

- Power dissipation in winding, \( P_w = V_w k_{cu} \frac{\pi}{4} (J_{rms})^2 = 3.2 \text{ Watts} \)
  - \( V_w = 12.3 \text{ cm}^3 \) (table of core characteristics)
  - \( k_{cu} = 0.3 \) (Leitz wire)
  - \( \frac{\pi}{4} \) at 100 \( ^\circ \text{C} \) (approx. max. \( T_s \)) = 2.2x10^{-8} ohm-m
  - \( J_{rms} = 4/(.64) = 6.25 \text{ A/mm}^2 \)

- Power dissipation in 3F3 ferrite core,
  \( P_{core} = V_c 1.5\times10^{-6} f^{1.3} (B_{ac})^{2.5} = 3.3 \text{ W} \)
  - \( B_{ac} \approx A_g \frac{N\sqrt{2}}{A_c \frac{\pi}{4}} I_{rms} = 0.18 \text{ mT}; \) assumes \( H_g >> H_{core} \)
  - \( A_g = (a + g)(d + g) = 1.71 \text{ cm}^2 \); \( g = 3\text{mm}/4 = .075 \text{ mm} \)
  - \( A_c = 1.5 \text{ cm}^2 \) (table of core characteristics)
  - \( V_c = 13.5 \text{ cm}^3 \) (table of core characteristics)
  - \( f = 100 \text{ kHz} \)
Analysis of a Specific Inductor Design (cont.)

- \[ L = \frac{N}{I} = 310 \text{ H} \]

- \[ \Phi = B_{ac} A_c = (0.18 \text{ T})(1.5 \times 10^{-4} \text{ m}^2) = 2.6 \times 10^{-5} \text{ Wb} \]

- Surface temperature \[ T_s = T_a + R_{\text{sa}} (P_w + P_{\text{core}}) = 104 \degree \text{C} \]

- \[ R_{\text{sa}} = R_{\text{rad}} \parallel R_{\text{conv}} = 9.8 \degree \text{C/W} \]

- \[ R_{\text{rad}} = \frac{60}{(5.1)(0.006)} \left[ \frac{373}{4} - \frac{313}{4} \right] = 20.1 \degree \text{C/W} \]

- \[ R_{\text{conv}} = \frac{4}{(1.34)(0.006)} \sqrt{\frac{0.035}{60}} = 19.3 \degree \text{C/W} \]

- Overcurrent of 25% (I= 5 amp rms) makes \[ T_s = 146 \degree \text{C} \]

- \[ P_w = (3.2 \text{ W})(1.25)^2 = 5 \text{ W} ; P_{\text{core}} = (3.3 \text{ W})(1.25)^{2.5} = 5.8 \text{ W} \]

- \[ T_s = (9.8 \degree \text{C/W})(10.8 \text{ W}) + 40 \degree \text{C} = 146 \degree \text{C} \]
Stored Energy Relation - Basis of Inductor Design

- Input specifications for inductor design
  - Inductance value $L$.
  - Rated peak current $I$.
  - Rated rms current $I_{\text{rms}}$.
  - Rated dc current (if any) $I_{\text{dc}}$.
  - Operating frequency $f$.
  - Maximum inductor surface temperature $T_s$ and maximum ambient temperature $T_a$.

- Design consists of the following:
  - Selection of core geometric shape and size
  - Core material
  - Winding conductor geometric shape and size
  - Number of turns in winding

- Design procedure starting point - stored energy relation
  - $[L I] I_{\text{rms}} = [N \Box] I_{\text{rms}}$
  - $N = \frac{k_{\text{cu}} A_W}{A_{\text{cu}}}$
  - $\Box = B A_{\text{core}}$; $I_{\text{rms}} = J_{\text{rms}} A_{\text{cu}}$
  - $L I I_{\text{rms}} = k_{\text{cu}} J_{\text{rms}} B A_W A_{\text{core}}$

- Equation relates input specifications (left-hand side) to needed core and winding parameters (right-hand side)

- A good design procedure will consist of a systematic, single-pass method of selecting $k_{cu}$, $J_{\text{rms}}$, $B$, $A_W$, and $A_{\text{core}}$.

**Goal:** Minimize inductor size, weight, and cost.
Core Database - Basic Inductor Design Tool

- Interactive core database (spreadsheet-based) key to a single pass inductor design procedure.
  - User enters input specifications from converter design requirements. Type of conductor for windings (round wire, Leitz wire, or rectangular wire or foil) must be made so that copper fill factor $k_{cu}$ is known.
  - Spreadsheet calculates capability of all cores in database and displays smallest size core of each type that meets stored energy specification.
  - Also can be designed to calculate (and display as desired) design output parameters including $J_{rms}$, $B$, $A_{cu}$, $N$, and air-gap length.
  - Multiple iterations of core material and winding conductor choices can be quickly done to aid in selection of most appropriate inductor design.

- Information on all core types, sizes, and materials must be stored on spreadsheet. Info includes dimensions, $A_w$, $A_{core}$, surface area of assembled inductor, and loss data for all materials of interest.

- Pre-stored information combined with user inputs to produce performance data for each core in spreadsheet. Sample of partial output shown below.

<table>
<thead>
<tr>
<th>Core No</th>
<th>Material</th>
<th>$AP = \frac{A_w A_{core}}{\text{cm}^4}$</th>
<th>$R_{q} \ [\text{T}=60 \ ^{\circ}\text{C}]$</th>
<th>$P_{sp} @ \ [\text{T}=60 \ ^{\circ}\text{C}]$</th>
<th>$J_{rms} @ \ [\text{T}=60 \ ^{\circ}\text{C}]$</th>
<th>$B_{ac} @ \ [\text{T}=60 \ ^{\circ}\text{C}]$</th>
<th>$k_{cu} J_{rms} \widehat{B} \cdot \frac{A_w A_{core}}{\text{cm}^4}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>3F3</td>
<td>2.1 cm$^4$</td>
<td>9.8 $^{\circ}$C/W</td>
<td>237 mW/cm$^3$</td>
<td>$3.3/\sqrt{k_{cu}}$</td>
<td>170 mT</td>
<td>$0.0125/\sqrt{k_{cu}}$</td>
</tr>
</tbody>
</table>
Details of Interactive Inductor Core Database Calculations

- User inputs: L, I, I_{rms}, I_{dc}, f, T_s, T_a, and k_{cu}

- Stored information (static, independent of converter requirements)
  - Core dimensions, A_w, A_{core}, V_c, V_w, surface area, mean turn length, mean magnetic path length, etc.
  - Quantitative core loss formulas for all materials of interest including approximate temperature dependence.

- Calculation of core capabilities (stored energy value)
  1. Compute converter-required stored energy value: L \cdot I \cdot I_{rms}.
  2. Compute allowable specific power dissipation \( P_{sp} = \frac{[T_s - T_a]}{R_{fsa}} \cdot [V_c + V_w] \). \( R_{fsa} = \frac{h}{A_s} \) or calculated interactively using input temperatures and formulas for convective and radiative heat transfer from Heat Sink chapter.
  3. Compute allowable flux density \( P_{sp} = k \cdot f^b \cdot \left[ B_{ac} \right]^d \) and current density \( P_{sp} = k_{cu} \cdot \left[ J_{rms} \right]^2 \).
  4. Compute core capabilities \( k_{cu} \cdot A_w \cdot A_{core} \cdot B \cdot J_{rms} \).

- Calculation of inductor design parameters.
  1. Area of winding conductor \( A_{cu} = \frac{I}{J_{rms}} \).
  2. Calculate skin depth \( \delta \) in winding. If \( A_{cu} > \delta \) at the operating frequency, then single round conductor cannot be used for winding.
    - Construct winding using Leitz wire, thin foils, or paralleled small dia. (\( \leq \delta \)) round wires.
3. Calculate number turns of $N$ in winding: $N = k_{cu} \frac{A_w}{A_{cu}}$.

4. Calculate air-gap length $L_g$. Air-gap length determined on basis that when inductor current equals peak value $I$, flux density equals peak value $B$.
   - Formulas for air-gap length different for different core types. Example for double-E core given in next slide.

5. Calculate maximum inductance $L_{\text{max}}$ that core can support. $L_{\text{max}} = N A_{\text{core}} \frac{B_{\text{peak}}}{I_{\text{peak}}}$.
   - If $L_{\text{max}} >$ required $L$ value, reduce $L_{\text{max}}$ by removing winding turns.
   - Save on copper costs, weight, and volume.
   - $P_w$ can be kept constant by increasing $P_{w,sp}$
   - Keep flux density $B_{\text{peak}}$ constant by adjusting gap length $L_g$.

6. Alternative $L_{\text{max}}$ reduction procedure, increasing the value of $L_g$, keeping everything else constant, is a poor approach. Would not reduce copper weight and volume and thus achieve cost savings. Full capability of core would not be utilized.
Setting Double-E Core Air-gap Length

- Set total airgap length $L_g$ so that $B_{\text{peak}}$ generated at the peak current $I_{\text{peak}}$.
- $L_g = N_g g$; $N_g =$ number of distributed gaps each of length $g$. Distributed gaps used to minimize amount of flux fringing into winding and thus causing additional eddy current losses.
- $R_m = \frac{N \frac{I_{\text{peak}}}{A_c} B_{\text{peak}}}{\frac{\mu_0 A_g}{A_c} B_{\text{peak}}}$
- $L_g = \frac{N \frac{I_{\text{peak}}}{\frac{\mu_0 A_g}{A_c} B_{\text{peak}}}}{A_c} = R_{m,\text{core}} + R_{m,\text{gap}} \approx R_{m,\text{gap}} = \frac{L_g}{\frac{\mu_0 A_g}{A_c} B_{\text{peak}}}$
- For a double-E core, $A_g = (a + \frac{L_g}{N_g}) (d + \frac{L_g}{N_g})$
  - $A_g \approx ad + (a + d) \frac{L_g}{N_g}$; $\frac{L_g}{N_g} << a$
- Insertion of expression for $A_g(L_g)$ into expression for $L_g(A_g)$ and solving for $L_g$ yields
  $$L_g = \frac{a}{\frac{B_{\text{peak}} A_c}{d \frac{\mu_0 N \frac{I_{\text{peak}}}{A_c}}{d N_g}} - \frac{a + d}{N_g}}$$
- Above expression for $L_g$ only valid for double-E core, but similar expressions can be developed for other core shapes.
Single Pass Inductor Design Procedure

Start

Enter design inputs into core database

Examine database outputs & select core

Neglect skin, proximity effects?

Yes

Select wires

No

Iterative selection of conductor type/size.

Estimate $L_{\text{max}}$. Too large?

Yes

Remove turns and readjust airgap

No

Finish
Inductor Design Example

- Assemble design inputs
  - \( L = 300 \text{ microhenries} \)
  - Peak current = 5.6 A, sinewave current, \( I_{\text{rms}} = 4 \text{ A} \)
  - Frequency = 100 kHz
  - \( T_s = 100 \degree\text{C} \); \( T_a = 40 \degree\text{C} \)

- Stored energy \( L I I_{\text{rms}} = (3 \times 10^{-4})(5.6)(4) \)
  = 0.00068 J-m\(^{-3}\)

- Core material and geometric shape
  - High frequency operation dictates ferrite material. 3F3 material has highest performance factor PF at 100 kHz.
  - Double-E core chosen for core shape.

- Double-E core with \( a = 1 \text{ cm} \) meets requirements.
  \[ k_{\text{cu}} J_{\text{rms}} B \geq 0.0125 \sqrt{k_{\text{cu}}} 0.0068 \]
  for \( k_{\text{cu}} > 0.3 \)

- Database output: \( R_D = 9.8 \degree\text{C/W} \) and
  \( P_{\text{sp}} = 237 \text{ mW/cm}^3 \)

- Core flux density \( B = 170 \text{ mT} \) from database. No \( I_{\text{dc}} \), \( B_{\text{peak}} = 170 \text{ mT} \).

- Winding parameters.
  - Litz wire used, so \( k_{\text{cu}} = 0.3 \). \( J_{\text{rms}} = 6 \text{ A/mm}^2 \)
  - \( A_{\text{cu}} = (4 \text{ A})/(6 \text{ A/mm}^2) = 0.67 \text{ mm}^2 \)
  - \( N = (140 \text{ mm}^2)((0.3)/(0.67 \text{ mm}^2)) = 63 \text{ turns} \).

- \( L_{\text{max}} = \frac{(63)(170 \text{ mT})(1.5 \times 10^{-4} \text{ m}^2)}{5.6 \text{ A}} \)
  \( \approx 290 \text{ microhenries} \)

- \( L_{\text{g}} = \frac{10^{-2}}{(0.17)(1.5 \times 10^{-4})}\)
  \( \frac{2.5 \times 10^{-2}}{(1.5 \times 10^{-2})(4\pi \times 10^{-7})(63)(5.6)} - (4)(1.5 \times 10^{-2}) \)
  \( L_{\text{g}} \approx 3 \text{ mm} \)

- \( L_{\text{max}} \approx L \) so no adjustment of inductance value is needed.
Iterative Inductor Design Procedure

- Iterative design procedure essentially consists of constructing the core database until a suitable core is found.

- Choose core material and shape and conductor type as usual.

- Use stored energy relation to find an initial area product $A_w A_c$ and thus an initial core size.
  - Use initial values of $J_{rms} = 2-4$ A/mm$^2$ and $B_{ac} = 50-100$ mT.

- Use initial core size estimate (value of a in double-E core example) to find corrected values of $J_{rms}$ and $B_{ac}$ and thus corrected value of $k_{cu} J_{rms} B A_w A_{core}$.

- Compare $k_{cu} J_{rms} B A_w A_{core}$ with $L I_{rms}$ and iterate as needed into proper size is found.
Simple, Non-optimal Inductor Design Method

- Assemble design inputs and compute required \( L I_{\text{rms}} \)

- Choose core geometry and core material based on considerations discussed previously.

- Assume \( J_{\text{rms}} = 2-4 \text{ A/mm}^2 \) and \( B_{\text{ac}} = 50-100 \text{ mT} \) and use \( LI_{\text{rms}} = k_{\text{cu}} J_{\text{rms}} B_{\text{ac}} A_w A_{\text{core}} \) to find the required area product \( A_w A_{\text{core}} \) and thus the core size.
  - Assumed values of \( J_{\text{rms}} \) and \( B_{\text{ac}} \) based on experience.

- Complete design of inductor as indicated.

- Check power dissipation and surface temperature using assumed values of \( J_{\text{rms}} \) and \( B_{\text{ac}} \). If dissipation or temperature are excessive, select a larger core size and repeat design steps until dissipation/temperature are acceptable.

- Procedure is so-called area product method. Useful in situations where only one or two inductors are to be built and size/weight considerations are secondary to rapid construction and testing.
Analysis of Specific Transformer Design

- Transformer specifications
  - Wound on double-E core with a = 1 cm using 3F3 ferrite.
  - \(I_{pri} = 4\) A rms, sinusoidal waveform; \(V_{pri} = 300\) V rms.
  - Frequency = 100 kHz
  - Turns ratio \(N_{pri}/N_{sec} = 4\) and \(N_{pri} = 32\).
  - Winding window split evenly between primary and secondary and wound with Litz wire.
  - Transformer surface black \((E = 0.9)\) and \(T_a \leq 40\) °C.
  - Find: core flux density, leakage inductance, and maximum surface temperature \(T_s\), and effect of 25% overcurrent on \(T_s\).

- Areas of primary and secondary conductors, \(A_{cu,pri}\) and \(A_{cu,sec}\).
  

\[
A_{w,pri} = \frac{N_{pri} A_{cu,pri}}{k_{cu,pri}}; \quad A_{w,sec} = \frac{N_{sec} A_{cu,sec}}{k_{cu,sec}}
\]

\[
A_{w,pri} + A_{w,sec} = A_w = \frac{N_{pri} A_{cu,pri}}{k_{cu}} + \frac{N_{sec} A_{cu,sec}}{k_{cu}}
\]

where \(k_{cu,pri} = k_{cu,sec} = k_{cu}\) since we assume primary and secondary are wound with same type of conductor.

- Equal power dissipation density in primary and secondary gives

\[
\frac{I_{pri}}{I_{sec}} = \frac{A_{cu,pri}}{A_{cu,sec}} = \frac{N_{sec}}{N_{pri}}
\]

- Using above equations yields \(A_{cu,pri} = \frac{k_{cu} A_w}{2 N_{pri}}\) and

\[
A_{cu,sec} = \frac{k_{cu} A_w}{2 N_{sec}}
\]

- Numerical values:

\[
A_{cu,pri} = \frac{(0.3)(140\ mm^2)}{(2)(32)} = 0.64\ mm^2
\]

and \(A_{cu,sec} = \frac{(0.3)(140\ mm^2)}{(2)(8)} = 2.6\ mm^2\)
Analysis of Specific Transformer Design (cont.)

- Power dissipation in winding $P_w = k_{cu} \rho_{cu} (J_{rms})^2 V_w$

- $J_{rms} = (4 \text{ A})/(0.64 \text{ mm}^2) = (16 \text{ A})/(2.6 \text{ mm}^2) = 6.2 \text{ A/mm}^2$

- $P_w = (0.3)(2.2 \times 10^{-8} \text{ ohm-m}) (6.2 \times 10^6 \text{ A/m}^2)^2 (1.23 \times 10^{-5} \text{ m}^3)$
  $P_w = 3.1 \text{ watts}$

- Flux density and core loss
  - $V_{pri,max} = N_{pri} A_c B_{ac} = (1.414)(300) = 425 \text{ V}$
  - $B_{ac} = \frac{425}{(32)(1.5 \times 10^{-4} \text{ m}^2)(2\pi)(10^5 \text{ Hz})} = 0.140 \text{ T}$
  - $P_{core} = (13.5 \text{ cm}^3)(1.5 \times 10^{-6})(100 \text{ kHz})^{1.3}(140 \text{ mT})^{2.5} = 1.9 \text{ W}$

- Leakage inductance $L_{leak} = \frac{\mu_0 (N_{pri})^2 b_w l_w}{3 h_w}$
  - $l_w = 8 \text{ a} = 8 \text{ cm}$
  - $L_{leak} = \frac{(4\pi \times 10^{-7})(32)^2(0.7)(10^{-2})(8 \times 10^{-2})}{(3)(2 \times 10^{-2})} \approx 12 \text{ microhenries}$

- Surface temperature $T_S$.
  - Assume $R_{\infty,sa} \approx 9.8 ^\circ \text{C/W}$.
  - Same geometry as inductor.
  - $T_S = (9.8)(3.1 + 1.9) + 40 = 89 ^\circ \text{C}$

- Effect of 25% overcurrent.
  - No change in core flux density.
  - Constant voltage applied to primary keeps flux density constant.
  - $P_w = (3.1)(1.25)^2 = 4.8 \text{ watts}$
  - $T_S = (9.8)(4.8 + 1.9) + 40 = 106 ^\circ \text{C}$
Sectioning of Transformer Windings to Reduce Winding Losses

- Reduce winding losses by reducing magnetic field (or equivalently the mmf) seen by conductors in winding. Not possible in an inductor.

- Simple two-section transformer winding situation.

- Division into multiple sections reduces MMF and hence eddy current losses.
Optimization of Solid Conductor Windings

- Normalized power dissipation:
  \[ \frac{P_w}{R_{dc,h}} = \frac{F_R R_{dc}}{R_{dc,h}} = (l_{rms})^2 \]

- Conductor height/diameter:
  \[ \frac{\sqrt{F_l}}{h} \]

- \( F_l = \) copper layer factor
  - \( F_l = b/b_o \) for rectangular conductors
  - \( F_l = d/d_o \) for round conductors

- \( h = \) effective conductor height
  - \( h = \sqrt{\frac{\pi}{4}} d \) for round conductors

- \( m = \) number of layers
Transformer Leakage Inductance

- Transformer leakage inductance causes overvoltages across power switches at turn-off.

- Leakage inductance caused by magnetic flux which does not completely link primary and secondary windings.

\[
H_{\text{window}} = H_{\text{leak}} = \frac{2 N_{\text{pri}} I_{\text{pri}} x}{h_w b_w} \quad ; \quad 0 < x < b_w/2
\]
\[
H_{\text{leak}} = \frac{2 N_{\text{pri}} I_{\text{pri}}}{h_w} (1 - x/b_w) \quad ; \quad b_w/2 < x < b_w
\]

- Linear variation of mmf in winding window indicates spatial variation of magnetic flux in the window and thus incomplete flux linkage of primary and secondary windings.

- If winding is split into \( p+1 \) sections, with \( p > 1 \), leakage inductance is greatly reduced.
Volt-Amp (Power) Rating - Basis of Transformer Design

- Input design specifications
  - Rated rms primary voltage $V_{pri}$
  - Rated rms primary current $I_{pri}$
  - Turns ratio $N_{pri}/N_{sec}$
  - Operating frequency $f$
  - Maximum temperatures $T_s$ and $T_a$
- Design consists of the following:
  - Selection of core geometric shape and size
  - Core material
  - Winding conductor geometric shape and size
  - Number of turns in primary and secondary windings.

- Design procedure starting point - transformer V-A rating $S$

\[
S = V_{pri} I_{pri} + V_{sec} I_{sec} = 2 V_{pri} I_{pri}
\]

\[
V_{pri} = N_{pri} \frac{d\phi}{dt} = \frac{N_{pri} A_{core} B_{ac}}{\sqrt{2}} ; I_{pri} = J_{rms} A_{cu,pri}
\]

\[
S = 2 V_{pri} I_{pri} = 2 \frac{N_{pri} A_{core} B_{ac}}{\sqrt{2}} J_{rms} A_{cu,pri}
\]

\[
A_{cu,pri} = \frac{k_{cu} A_w}{2 N_{pri}}
\]

\[
S = 2 V_{pri} I_{pri} = 2 \frac{N_{pri} A_{core} B_{ac}}{\sqrt{2}} J_{rms} \frac{k_{cu} A_w}{2 N_{pri}}
\]

\[
S = V_{pri} I_{pri} = 4.4 k_{cu} f A_{core} A_w J_{rms} B_{ac}
\]

- Equation relates input specifications (left-hand side) to core and winding parameters (right-hand side).

- Desired design procedure will consist of a systematic, single-pass method of selecting $k_{cu}, A_{core}, A_w, J_{rms},$ and $B_{ac}$.
Core Database - Basic Transformer Design Tool

- Interactive core database (spreadsheet-based) key to a single pass transformer design procedure.
  - User enters input specifications from converter design requirements. Type of conductor for windings (round wire, Leitz wire, or rectangular wire or foil) must be made so that copper fill factor $k_{cu}$ is known.
  - Spreadsheet calculates capability of all cores in database and displays smallest size core of each type that meets $V-I$ specification.
  - Also can be designed to calculate (and display as desired) design output parameters including $J_{rms}$, $B$, $A_{cu, pri}$, $A_{cu, sec}$, $N_{pri}$, $N_{sec}$, and leakage inductance.
- Multiple iterations of core material and winding conductor choices can be quickly done to aid in selection of most appropriate transformer design.
- Information on all core types, sizes, and materials must be stored on spreadsheet. Info includes dimensions, $A_{w}$, $A_{core}$, surface area of assembled transformer, and loss data for all materials of interest.
- Pre-stored information combined with user inputs to produce performance data for each core in spreadsheet. Sample of partial output shown below.

<table>
<thead>
<tr>
<th>Core No.</th>
<th>Material</th>
<th>$AP = A_{w}A_{c}$</th>
<th>$R[]$ $T=60$ °C</th>
<th>$P_{sp}$ @ $T_s=100$ °C</th>
<th>$J_{rms}$ @ $T_s=100$ °C &amp; $P_{sp}$</th>
<th>$\hat{B}_{rated}$ @ $T_s=100$ °C &amp; 100 kHz</th>
<th>$2.22 k_{cu}f J_{rms} \hat{B}$ AP</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>3F3</td>
<td>2.1 cm$^4$</td>
<td>9.8 °C/W</td>
<td>237 mW/cm$^3$</td>
<td>170 mT</td>
<td>$\sqrt{\frac{k_{cu}R_{dc}}{R_{ac}}} \sqrt{\frac{A}{mm^2}}$</td>
<td>$\sqrt{\frac{k_{cu}R_{dc}}{R_{ac}}} [V-A]$</td>
</tr>
</tbody>
</table>
Details of Interactive Transformer Core Database Calculations

- User inputs: $V_{pri}$, $I_{pri}$, turns ratio $N_{dc}/N_{sec}$, $f$, $T_s$, $T_a$, and $k_{cu}$

- Stored information (static, independent of converter requirements)
  - Core dimensions, $A_w$, $A_{core}$, $V_c$, $V_w$, surface area, mean turn length, mean magnetic path length, etc.
  - Quantitative core loss formulas for all materials of interest including approximate temperature dependence.

- Calculation of core capabilities
  1. Compute converter-required stored energy value: $S = 2 V_{pri} I_{pri}$
  2. Compute allowable specific power dissipation $P_{sp} = \left[ T_s - T_a \right] / \left( R_{hsa} [V_c + V_w] \right)$. $R_{hsa} = h/A_s$ or calculated interactively using input temperatures and formulas for convective and radiative heat transfer from Heat Sink chapter.
  3. Compute allowable flux density $P_{sp} = k_{fb} [B_{ac}]^d$ and current density $P_{sp} = k_{cu} \Box_{cu} \{J_{rms}\}^2$.
  4. Compute core capabilities $4.4 f k_{cu} A_w A_{core} B_{ac} J_{rms}$

- Calculation transformer parameters.
  1. Calculate number of primary turns $N_{pri} = V_{pri} / \{2\pi f A_{cpre} B_{ac}\}$ and secondary turns $N_{sec} = V_{sec} / \{2\pi f A_{cpre} B_{ac}\}$
  2. Calculate winding conductor areas assuming low frequencies or use of Leitz wire
     - $A_{cu,pri} = [k_{cu} A_w] / [2 N_{pri}]$ and $A_{cu,sec} = [k_{cu} A_w] / [2 N_{sec}]$
3. Calculate winding areas assuming eddy current/proximity effect is important

- Only solid conductors, round wires or rectangular wires (foils), used. \( J_{\text{rms}} = \left\{ \frac{P_{\text{sp}} R_{\text{dc}}}{R_{\text{ac}} k_{\text{cu}} r_{\text{cu}}} \right\}^{1/2} \)
- Conductor dimensions must simultaneously satisfy area requirements and requirements of normalized power dissipation versus normalized conductor dimensions.
- May require change in choice of conductor shape. Most likely will require choice of foils (rectangular shapes).
- Several iterations may be needed to find proper combinations of dimensions, number of turns per layer, and number of layers and sections.
- Best illustrated by a specific design example.

4. Estimate leakage inductance \( L_{\text{leak}} = \left\{ \mu_0 N_{\text{pri}} \right\}^2 l_w b_w / \{3 \ p^2 h_w \} \)

5. Estimate \( S_{\text{max}} = 4.4 k_{\text{cu}} f A_{\text{core}} A_w J_{\text{rms}} B_{\text{ac}} \)

6. If \( S_{\text{max}} > S = 2 V_{\text{pri}} I_{\text{pri}} \) reduce \( S_{\text{max}} \) and save on copper cost, weight, and volume.
   - If \( N_{\text{pri}} w A_c B_{\text{ac}} > V_{\text{pri}} \), reduce \( S_{\text{max}} \) by reducing \( N_{\text{pri}} \) and \( N_{\text{sec}} \).
   - If \( J_{\text{rms}} A_{\text{cu, pri}} > I_{\text{rms}} \), reduce \( A_{\text{cu, pri}} \) and \( A_{\text{cu, sec}} \).
   - If \( S > S_{\text{max}} \) by only a moderate amount (10-20%) and smaller than \( S_{\text{max}} \) of next core size, increase \( S_{\text{max}} \) of present core size.
   - Increase \( I_{\text{rms}} \) (and thus winding power dissipation) as needed. Temperature \( T_s \) will increase a modest amount above design limit, but may be preferable to going to larger core size.
Single Pass Transformer Design Procedure

Start

Enter design inputs into core database

Examine database outputs & select core

Neglect skin, proximity effects?

Yes
Select wires

No
Iterative selection of conductor type/size.

Estimate $S_{\text{max}}$

Too large?

No

Remove turns

Yes

Finish
Transformer Design Example

• Design inputs
  • $V_{pri} = 300$ V rms ; $I_{rms} = 4$ A rms
  • Turns ratio $n = 4$
  • Operating frequency $f = 100$ kHz
  • $T_s = 100$ °C and $T_a = 40$ °C

• $V - I$ rating $S = (300$ V rms$)(4$ A rms$) = 1200$ watts

• Flux density and number of primary and secondary turns.
  • From core database, $B_{ac} = 170$ mT.
  • $N_{pri} = \frac{300 \sqrt{2}}{(1.5 \times 10^{-4} m^2)(2\pi)(10^5 Hz)(0.17 T)} = 26.5 \approx 24$. Rounded down to 24 to increase flexibility in designing sectionalized transformer winding.
  • $N_{sec} = \frac{24}{6} = 6$.

• Core volt-amp rating $= 2,600 \sqrt{k_{cu} \sqrt{R_{dc} \over R_{ac}}}$
  • Use solid rectangular conductor for windings because of high frequency. Thus $k_{cu} = 0.6$ and $R_{ac}/R_{dc} = 1.5$.
  • Core volt-amp capability $= 2,600 \sqrt{0.6 \over 1.5} = 1644$ watts. > 1200 watt transformer rating. Size is adequate.

• Using core database, $R_{\square} = 9.8$ °C/W
  and $P_{sp} = 240$ mW/cm$^3$.

• Core material, shape, and size.
  • Use 3F3 ferrite because it has largest performance factor at 100 kHz.
  • Use double-E core. Relatively easy to fabricate winding.

• From core database $J_{rms} = \frac{3.3}{\sqrt{(0.6)(1.5)}} = 3.5$ A/mm$^2$.
  • $A_{cu,pri} = \frac{4 \text{ A rms}}{3.5 \text{ A rms/mm}^2} = 1.15 \text{ mm}^2$
  • $A_{cu,sec} = (4)(1.15 \text{ mm}^2) = 4.6 \text{ mm}^2$
Transformer Design Example (cont.)

- Primary and secondary conductor areas - proximity effect/eddy currents included. Assume rectangular (foil) conductors with \( k_{cu} = 0.6 \) and layer factor \( F_1 = 0.9 \).

- Iterate to find compatible foil thicknesses and number of winding sections.
- 1st iteration - assume a single primary section and a single secondary section and each section having single turn per layer. Primary has 24 layers and secondary has 6 layers.

- Primary layer height \( h_{pri} = \frac{A_{cu,pri}}{F_1 h_w} = 1.15 \text{ mm}^2 (0.9)(20 \text{ mm}) = 0.064 \text{ mm} \)

- Normalized primary conductor height \( \bar{\eta} = \frac{\sqrt{F_1} h_{pri}}{d} = \frac{\sqrt{0.9} (0.064 \text{ mm})}{(0.24 \text{ mm})} = 0.25 \); \( \bar{\eta} = 0.24 \text{ mm} \) in copper at 100 kHz and 100 °C.

- Optimum normalized primary conductor height \( \bar{\eta} = 0.3 \) so primary winding design is satisfactory.

- Secondary layer height \( h_{sec} = \frac{A_{cu,sec}}{F_1 h_w} = \frac{4.6 \text{ mm}^2}{(0.9)(20 \text{ mm})} \approx 0.26 \text{ mm} \).

- Normalized secondary conductor height \( \bar{\eta} = \frac{\sqrt{F_1} h_{sec}}{d} = \frac{\sqrt{0.9} (0.26 \text{ mm})}{(0.24 \text{ mm})} = 1 \)

- However a six layer section has an optimum \( \bar{\eta} = 0.6 \). A two layer section has an optimum \( \bar{\eta} = 1 \). 2nd iteration needed.

- 2nd iteration - sectionalize the windings.

- Use a secondary of 3 sections, each having two layers, of height \( h_{sec} = 0.26 \text{ mm} \).

- Secondary must have single turn per layer. Two turns per layer would require \( h_{sec} = 0.52 \text{ mm} \) and thus \( \bar{\eta} = 2 \). Examination of normalized power dissipation curves shows no optimum \( \bar{\eta} = 2 \).
Transformer Design Example (cont.)

Three secondary sections requires four primary sections.

- Two outer primary sections would have $24/6 = 4$ turns each and the inner two sections would have $24/3 = 8$ turns each.
- Need to determine number of turns per layer and hence number of layers per section.

<table>
<thead>
<tr>
<th>Turns/layer</th>
<th>$h_{pri}$</th>
<th>No. of Layers</th>
<th>$f$</th>
<th>Optimum $f$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.064 mm</td>
<td>8</td>
<td>0.25</td>
<td>0.45</td>
</tr>
<tr>
<td>2</td>
<td>0.128 mm</td>
<td>4</td>
<td>0.5</td>
<td>0.6</td>
</tr>
<tr>
<td>3</td>
<td>0.26 mm</td>
<td>2</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

- Use four turns per layer. Two interior primary sections have two layers and optimum value of $f$. Two outer sections have one layer each and $f$ not optimum, but only results in slight increase in loss above the minimum.

- Leakage inductance $L_{\text{leak}}$

$$L_{\text{leak}} = \frac{(4\pi \times 10^{-9})(24)^2(8)(0.7)(1)}{(3)(6)^2(2)} = 0.2 \text{ mH}$$

- Sectionalizing increases capacitance between windings and thus lowers the transformer self-resonant frequency.

- $S_{\text{max}} = 1644$ watts

- Rated value of $S = 1200$ watts only marginally smaller than $S_{\text{max}}$. Little to be gained in reducing $S_{\text{max}}$ to $S$ unless a large number of transformer of this design are to be fabricated.

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Iterative Transformer Design Procedure

- Iterative design procedure essentially consists of constructing the core database until a suitable core is found.

- Choose core material and shape and conductor type as usual.

- Use V - I rating to find an initial area product $A_w A_c$ and thus an initial core size.

  - Use initial values of $J_{rms} = 2-4 \text{ A/mm}^2$ and $B_{ac} = 50-100 \text{ mT}$.

  - Use initial core size estimate (value of a in double-E core example) to find corrected values of $J_{rms}$ and $B_{ac}$ and thus corrected value of $4.4 f k_{cu} J_{rms} \hat{B} A_w A_c$.

  - Compare $4.4 f k_{cu} J_{rms} \hat{B} A_w A_c$ with $2 V_{pri} I_{pri}$ and iterate as needed into proper size is found.
Simple, Non-optimal Transformer Design Method

- Assemble design inputs and compute required $2 V_{pri} I_{pri}$

- Choose core geometry and core material based on considerations discussed previously.

- Assume $J_{rms} = 2-4$ A/mm² and $B_{ac} = 50-100$ mT and use $2 V_{pri} I_{pri} = 4.4 f k_{cu} J_{rms} B_{ac} A_w A_{core}$ to find the required area product $A_w A_{core}$ and thus the core size.
  - Assumed values of $J_{rms}$ and $B_{ac}$ based on experience.

- Complete design of transformer as indicated.

- Check power dissipation and surface temperature using assumed values of $J_{rms}$ and $B_{ac}$. If dissipation or temperature are excessive, select a larger core size and repeat design steps until dissipation/temperature are acceptable.

- Procedure is so-called area product method. Useful in situations where only one or two transformers are to be built and size/weight considerations are secondary to rapid construction and testing.